



## PRODUCT SPECIFICATION

- Tentative Specification
- Preliminary Specification
- Approval Specification

**MODEL NO.: V546HK3**

**SUFFIX: LS5**

**Ver. C7**

**Customer:**

APPROVED BY

SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	YI-CHEN Chiang

**CONTENTS**

REVISION HISTORY .....	4
1. GENERAL DESCRIPTION .....	5
1.1 OVERVIEW .....	5
1.2 FEATURES .....	5
1.3 APPLICATION .....	5
1.4 GENERAL SPECIFICATIONS .....	5
1.5 MECHANICAL SPECIFICATIONS .....	6
2. ABSOLUTE MAXIMUM RATINGS .....	7
2.1 ABSOLUTE RATINGS OF ENVIRONMENT .....	7
2.2 ELECTRICAL ABSOLUTE RATINGS .....	8
2.2.1 TFT LCD MODULE .....	8
2.2.2 BACKLIGHT CONVERTER UNIT .....	8
3. ELECTRICAL CHARACTERISTICS .....	9
3.1 TFT LCD MODULE .....	9
3.2 BACKLIGHT UNIT .....	12
3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C) .....	12
3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C) .....	12
Note (6) Below diagram is only for power supply design reference. ....	13
3.2.3 CONVERTER INTERFACE CHARACTERISTICS .....	14
4. BLOCK DIAGRAM OF INTERFACE .....	16
4.1 TFT LCD MODULE .....	16
5. INPUT TERMINAL PIN ASSIGNMENT .....	17
5.1 TFT LCD MODULE .....	17
Note (11) Please reference Appendix A .....	21
5.2 BACKLIGHT UNIT .....	22
5.3 DRIVING BOARD UNIT .....	23
5.4 BLOCK DIAGRAM OF INTERFACE .....	24
5.5 LVDS INTERFACE .....	25
5.6 COLOR DATA INPUT ASSIGNMENT .....	27
6. INTERFACE TIMING .....	28

6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C).....	28
6.1.1 Timing spec for Frame Rate = 50Hz .....	28
6.1.2 Timing spec for Frame Rate = 60Hz .....	29
6.2 POWER ON/OFF SEQUENCE.....	33
6.2.1 POWER ON/OFF SEQUENCE.....	33
6.2.2 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON .....	34
 7. OPTICAL CHARACTERISTICS .....	35
7.1 TEST CONDITIONS.....	35
7.2 OPTICAL SPECIFICATIONS .....	36
 8. DEFINITION OF LABELS.....	42
8.1 CMI MODULE LABEL .....	42
 9. Packaging .....	43
9.1 PACKING SPECIFICATIONS.....	43
9.2 PACKING METHOD.....	43
 10. Internal Standart .....	45
10.1 ASSEMBLY AND HANDLING PRECAUTIONS .....	45
10.2 EMC .....	45
 11. PRECAUTIONS .....	46
11.1 ASSEMBLY AND HANDLING PRECAUTIONS .....	46
11.2 SAFETY PRECAUTIONS.....	46
 12. MECHANICAL CHARACTERISTIC .....	47
Appendix A .....	50

## REVISION HISTORY

Version	Date	Page (New)	Section	Description
A1	Oct. 14,11	all	all	Tentative Specification Ver 0.0 was first issued.
B1	Nov.10,11	all	all	Preliminary Specification Ver1.0 was first issued.
B1	Dec.22,11	9 36 47	3.1 7.2 12	Update electrical characteristic Update optical specification Update mechanical characteristic
C7	Feb.07,12	1 13	3.2.2	Update ver. C7 Update power supply reference diagram
C7	Feb.29,12	12	3.2	Modify Light Bar and Converter Characteristic

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V546HK3-LS5 is a 54.6" TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit). The driving board module for backlight is built-in.

### 1.2 FEATURES

- High brightness 400nits
- High contrast ratio 5000:1
- Fast response time Gray to Gray typical 6ms
- High color saturation 72% NTSC
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance

### 1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1209.6(H) x 680.4(V) (54.6" diagonal)	mm	(1)
Bezel Opening Area	1217.6 (H) x 688.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.21(H) x 0.63(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 3.5%), Hardness 3H	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.



# PRODUCT SPECIFICATION

## 1.5 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1235.9	1237.4	1238.9	mm Module Size
	Vertical (V)	709.8	711.3	712.8	mm
	Depth (D)	16.4	18.4	19.4	mm To Rear
	Weight	23	24	25	mm To converter cover
		16300	16800	17200	g Weight

Note (1)Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	$T_{ST}$	-20	+60	°C	(1)
Operating Ambient Temperature	$T_{OP}$	0	50	°C	(1), (2)
Shock (Non-Operating)	$S_{NOP}$	$\pm X, \pm Y$ $\pm Z$	- 30 30	G	(3), (5)
Vibration (Non-Operating)	$V_{NOP}$	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.

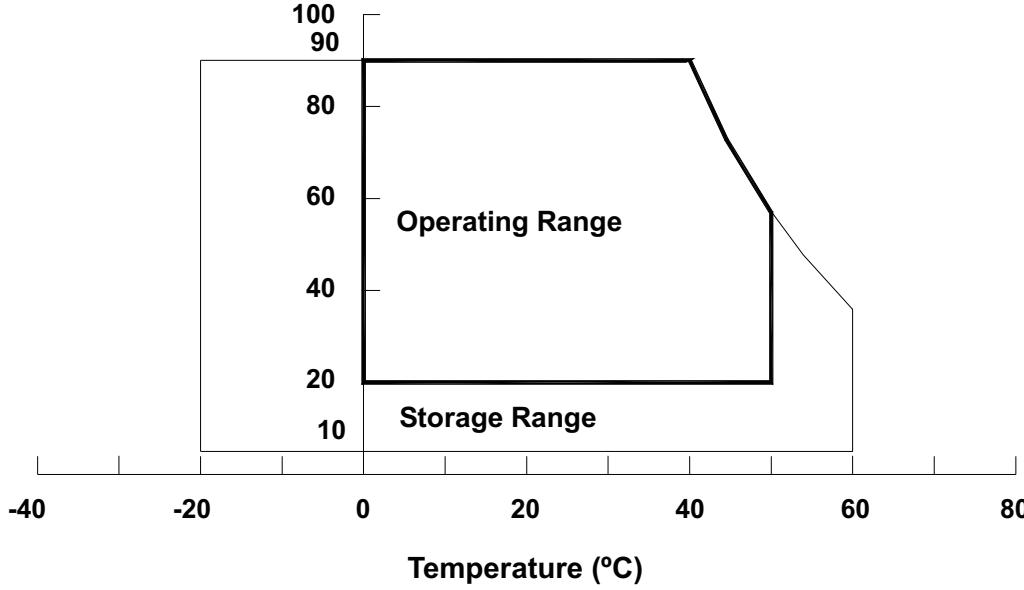
Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X, \pm Y, \pm Z$ .

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Relative Humidity (%RH)



## 2.2 ELECTRICAL ABSOLUTE RATINGS

## 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	$V_{CC}$	-0.3	13.5	V	(1)
Logic Input Voltage	$V_{IN}$	-0.3	3.6	V	

## 2.2.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	$V_W$	$T_a = 25^\circ C$	-	-	60	$V_{RMS}$	3D Mode
Converter Input Voltage	$V_{BL}$	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

## 3. ELECTRICAL CHARACTERISTICS

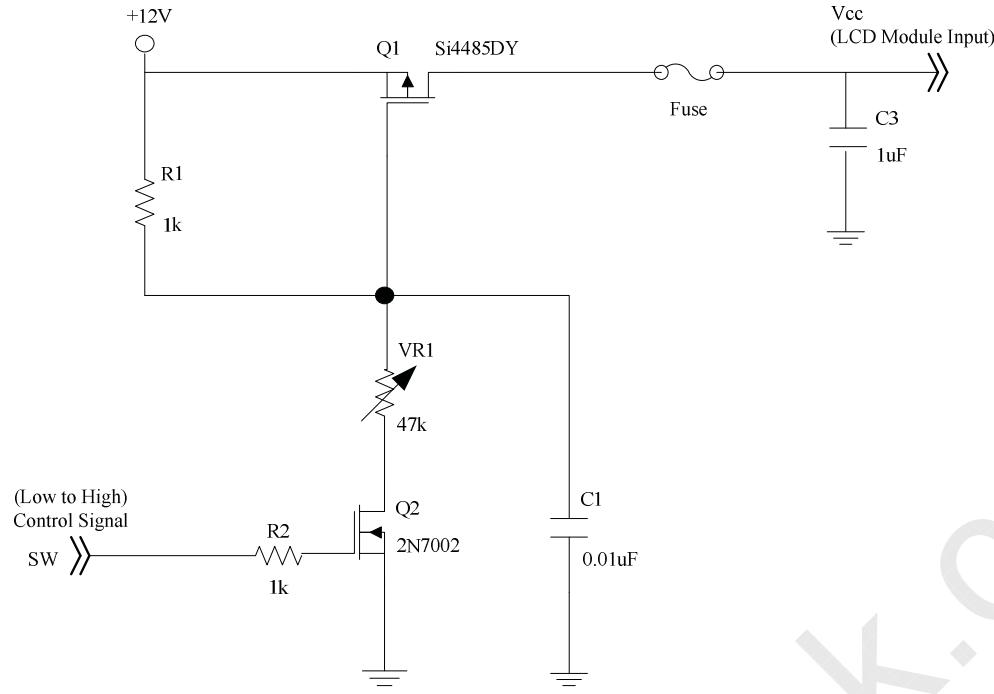
## 3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

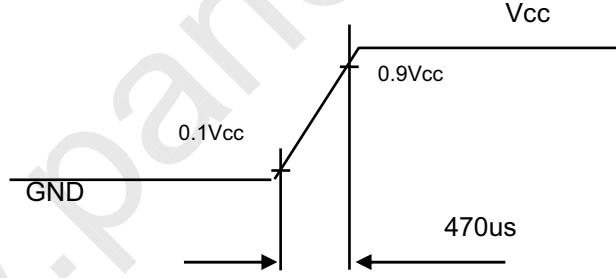
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current	I <sub>RUSH</sub>	—	—	2.67	A	(2)
Power Consumption	White Pattern	—	—	9.36	11.52	W
	Horizontal Stripe	—	—	19.92	24	W
	Black Pattern	—	—	8.88	10.8	W
Power Supply Current	White Pattern	—	—	0.78	0.96	A
	Horizontal Stripe	—	—	1.66	2	A
	Black Pattern	—	—	0.74	0.9	A
LVDS interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	—	—	mV
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	—	—	-100	mV
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V
	Differential input voltage (single-end)	V <sub>ID</sub>	200	—	600	mV
	Terminating Resistor	R <sub>T</sub>	—	100	—	ohm
CMIS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	—	3.3	V
	Input Low Threshold Voltage	V <sub>IL</sub>	0	—	0.7	V

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 120\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



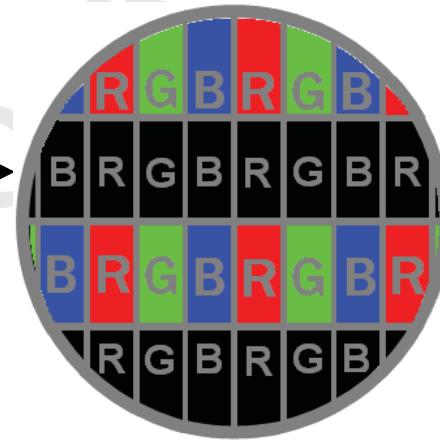
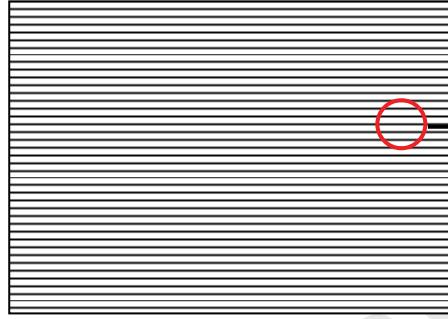
Active Area

b. Black Pattern

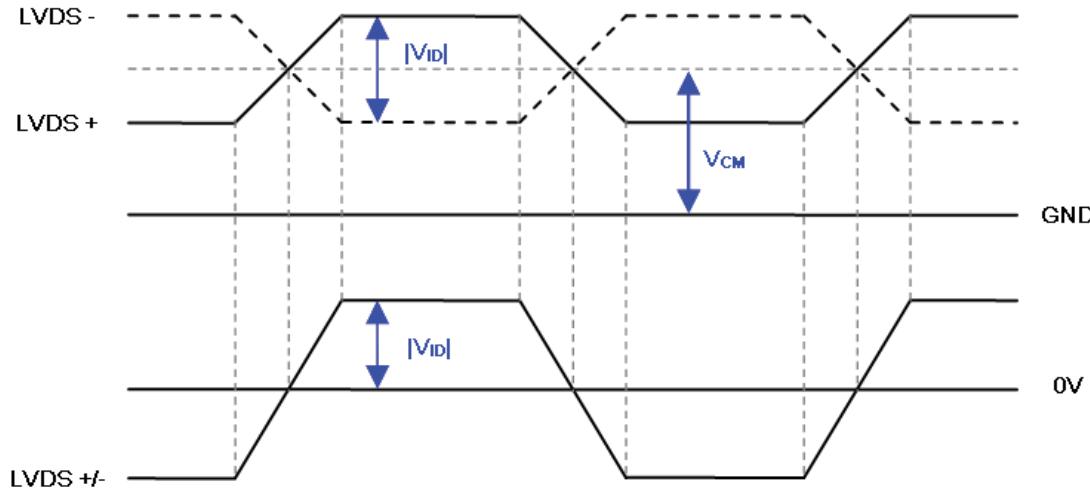


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



### 3.2 BACKLIGHT UNIT

#### 3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current (16 String)	I <sub>f</sub>	-	1840	1950.4	mA	
One String Current	I <sub>L(2D)</sub>	-	115	121.9	mA	
	I <sub>L(3D)</sub>	-	450	477	mApeak	3D ENA=ON
LED Forward Voltage	V <sub>f</sub>	5.7	6.1	6.4	V <sub>DC</sub>	I <sub>L</sub> =115mA
One String Voltage	V <sub>w</sub>	45.6	-	51.2	V <sub>DC</sub>	I <sub>L</sub> =115mA
One String Voltage Variation	△V <sub>w</sub>	-	-	2	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, I<sub>L</sub> =115mA.

#### 3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL(2D)</sub>	-	100	115	W	(1), (2) IL = 115 mA
	P <sub>BL(3D)</sub>	-	97.3	114	W	(1), (2) IL=450mA.
Converter Input Voltage	V <sub>BL</sub>	22.8	24.0	25.2	V <sub>DC</sub>	
Converter Input Current	I <sub>BL(2D)</sub>	-	4.17	4.79	A	Non Dimming
	I <sub>BL(3D)</sub>	-	4	4.75	A	
Input Inrush Current	I <sub>R(2D)</sub>	-	-	6.49	Apeak	V <sub>BL</sub> =22.8V,(IL=typ.) (3), (6)
	I <sub>R(3D)</sub>	-	-	11	Apeak	V <sub>BL</sub> =22.8V,(IL=450mA.)(3), (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Minimum Duty Ratio	D <sub>MIN</sub>	5	10	-	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption  $P_{BL}$ . Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 55" backlight unit under input voltage 24V, average LED current 121.9mA at 2D Mode (LED current 477 mA<sub>peak</sub> at 3D Mode) and lighting 1 hour later.

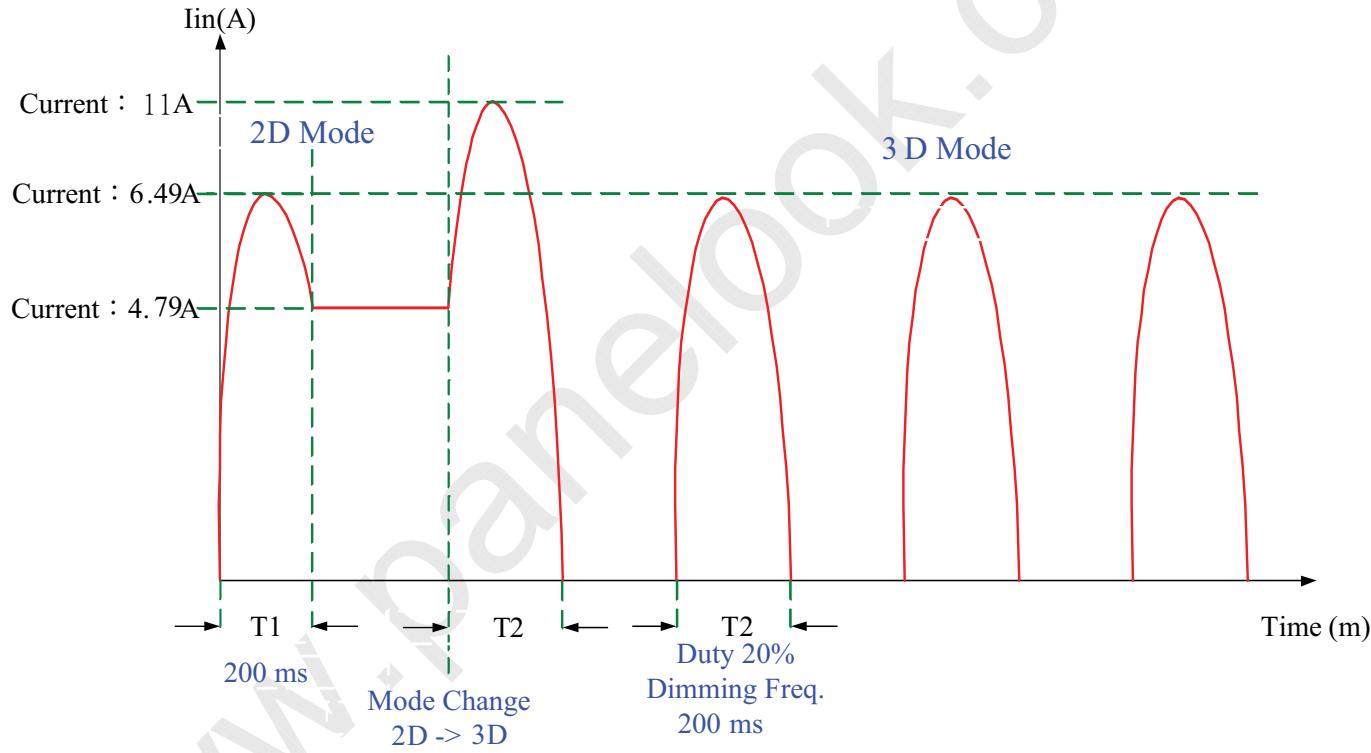
Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

Note (5) FB and DMIN are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.

**Test Condition:  $V_{BL}=22.8V$ ,  $IL=115mA$  at 2D Mode/  $IL=(450)mA$ peak at 3D Mode**



## 3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter	Symbol	Test Condition	Value			Unit	Note
			Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.5	V
	OFF		—	0	—	0.8	V
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V
	LO		—	0	—	0.8	V
External PWM Control Frequency	FEPWM	—	150	160	170	Hz	Normal mode
Error Signal	ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)
VBL Rising Time	Tr1	—	30	—	—	ms	10%-90%V <sub>BL</sub>
Control Signal Rising Time	Tr	—	—	—	100	ms	
Control Signal Falling Time	Tf	—	—	—	100	ms	
PWM Signal Rising Time	TPWMR	—	—	—	100	us	(6)
PWM Signal Falling Time	TPWMF	—	—	—	100	us	
Input Impedance	Rin	—	1	—	—	MΩ	EPWM, BLON
PWM Delay Time	TPWM	—	100	—	300	ms	(6)
BLON Delay Time	T <sub>on</sub>	—	300	—	500	ms	
	T <sub>on1</sub>	—	300	—	500	ms	
BLON Off Time	Toff	—	300	—	500	ms	

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.

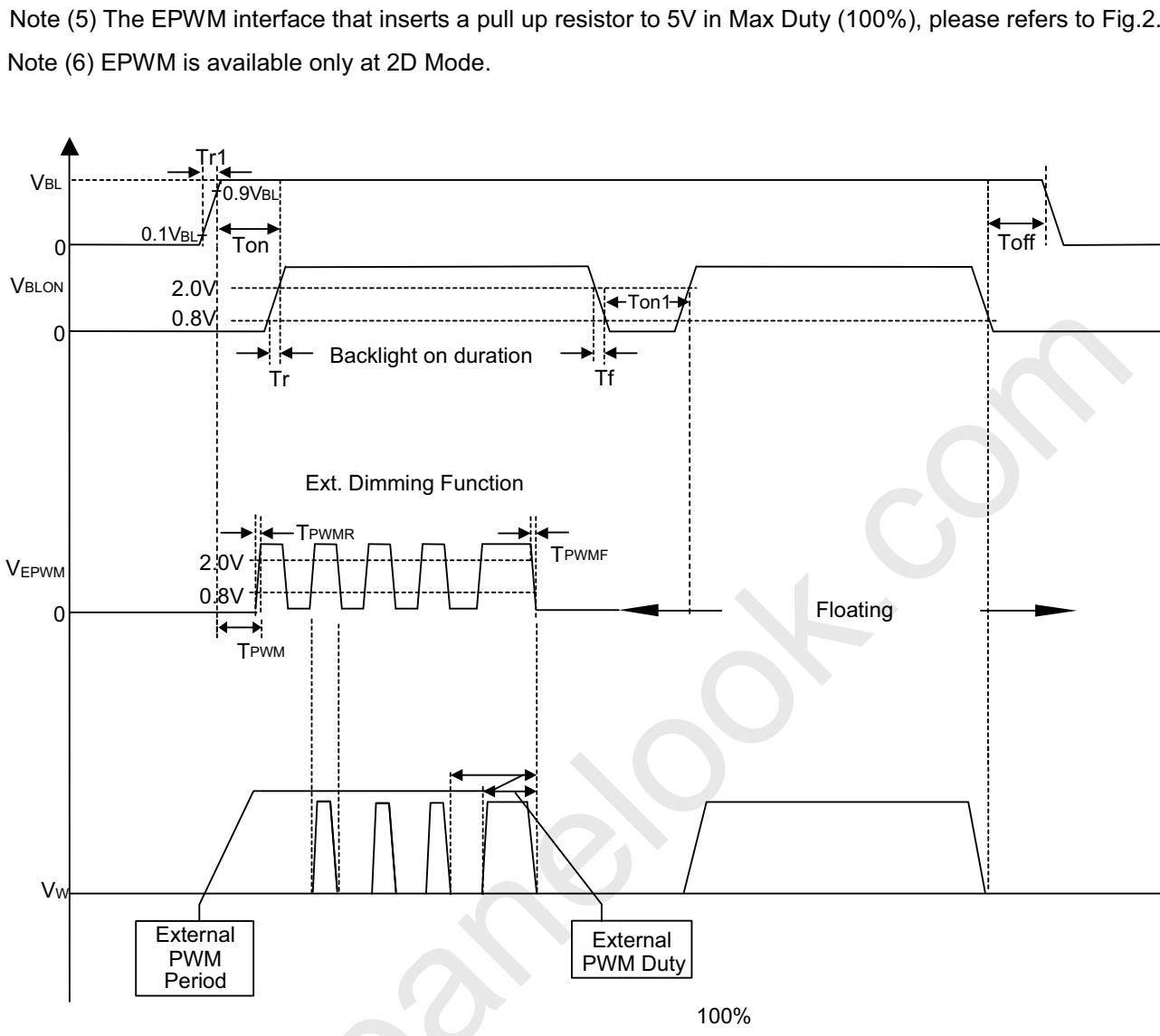


Fig. 1

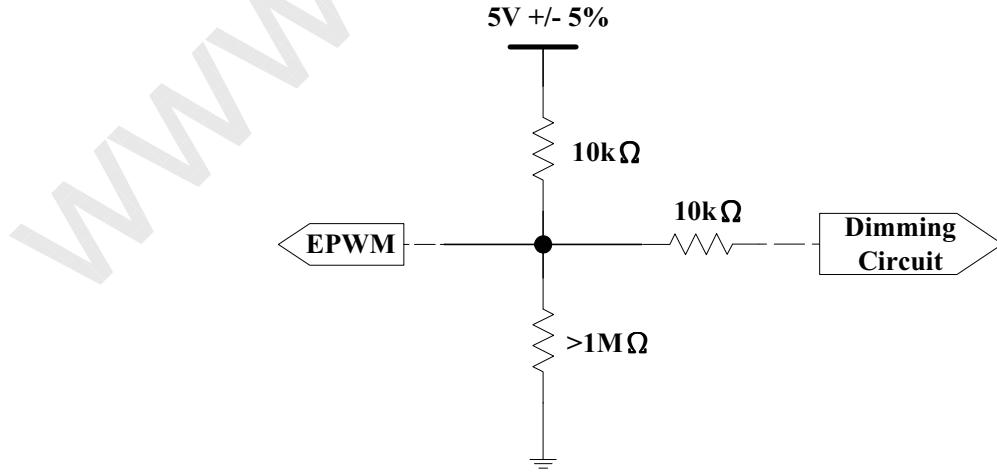
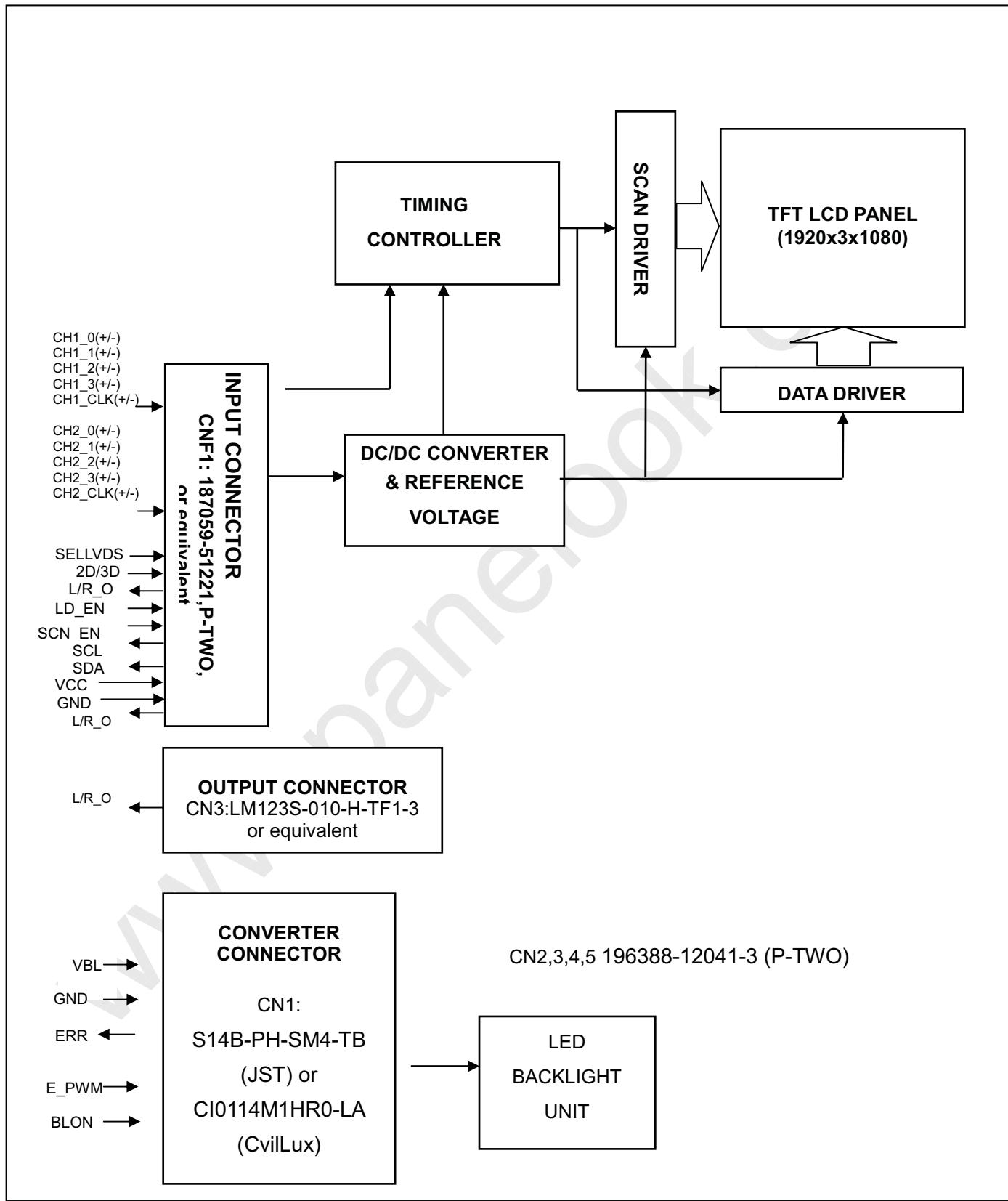


Fig. 2

## 4. BLOCK DIAGRAM OF INTERFACE

## 4.1 TFT LCD MODULE



## 5 .INPUT TERMINAL PIN ASSIGNMENT

### 5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment: (187059-51221 (P-TWO) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	I2C Serial Clock (for 3D format selection function)	(11)
3	SDA	I2C Serial Data (for 3D format selection function)	
4	N.C.	No Connection	(1)
5	L/R_O	Output signal for Left Right Glasses control	(10)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)(7)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(9)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input	(9)
20	OCLK+	Odd pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(9)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)(8)
27	L/R	Input signal for Left Right eye frame synchronous(Frame sequence mode)	(4)(8)

28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(9)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	(9)
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	(9)
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	LD_EN	Input signal for Local Dimming Enable	(5)(8)
43	SCN_EN	Input signal for Scanning Enable	(6)(8)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	(1)
47	N.C.	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CN3 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(10)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

$V_{IL}=0\sim0.8$  V,  $V_{IH}=2.0\sim3.3$  V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) Local dimming enable selection.

L= Connect to GND , H=Connect to +3.3V or open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

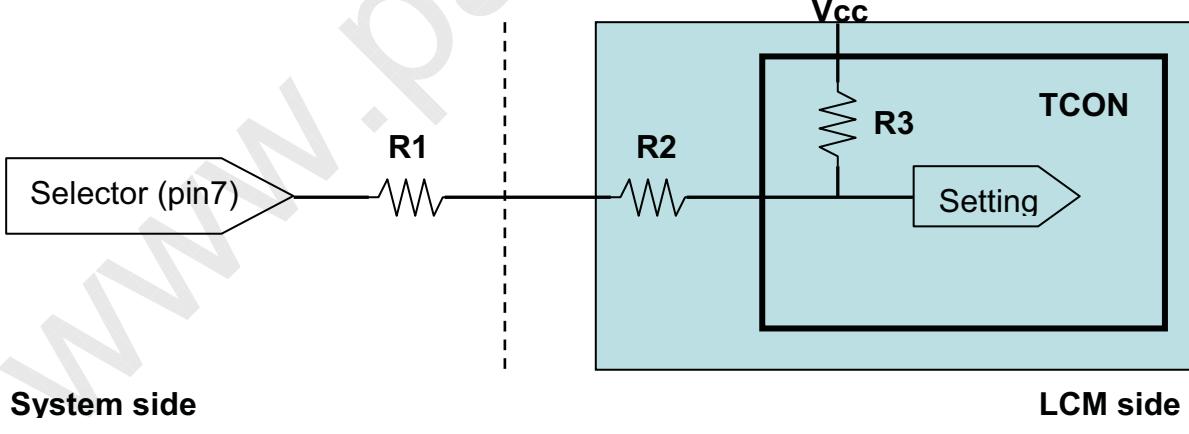
Note (6) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

Note (7) SELLVDS LD\_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ( $R1 < 1K$  Ohm)



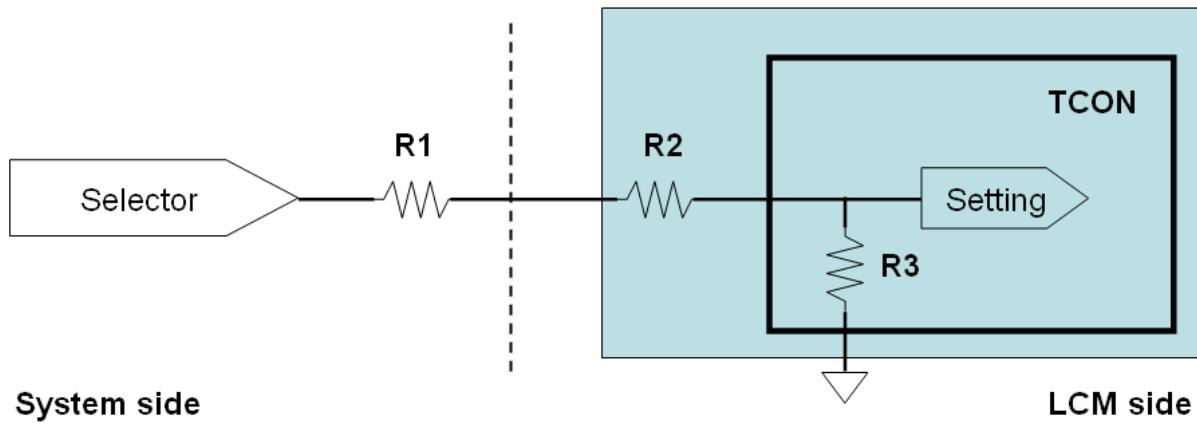
System side

System side

$R1 < 1K$

Note (8) 2D/3D, L/R, and SCN\_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ( $R1 < 1K$  Ohm)



System side:  $R1 < 1K$

Note (9) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

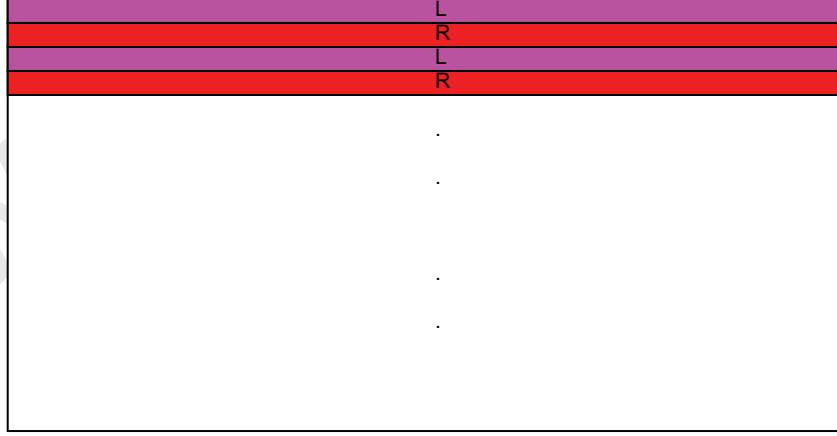
Note (10) The definition of L/R\_O signal as follows

$L = 0V$ ,  $H = +3.3V$

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

Note (11) Please reference Appendix A

Note (12) Currently, we only support line alternative format (1<sup>st</sup> line is left signal), show as the attached block diagram. In the future, we will support other format.



Line alternative format

## 5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2,3,6,7: 196388-12041-3 (P-TWO)

Pin №	Symbol	Feature
1	VLED	Positive of LED String
2	VLED	
3	VLED	
4	VLED	
5	NC	NC
6	NC	
7	NC	
8	NC	
9	N1	Negative of LED String
10	N2	
11	N3	
12	N4	

Note (1)The backlight interface housing for high voltage side is a model 51281-1094, manufactured by Molex or equivalent. The mating header on converter part number is 51281-1094

## 5.3 DRIVING BOARD UNIT

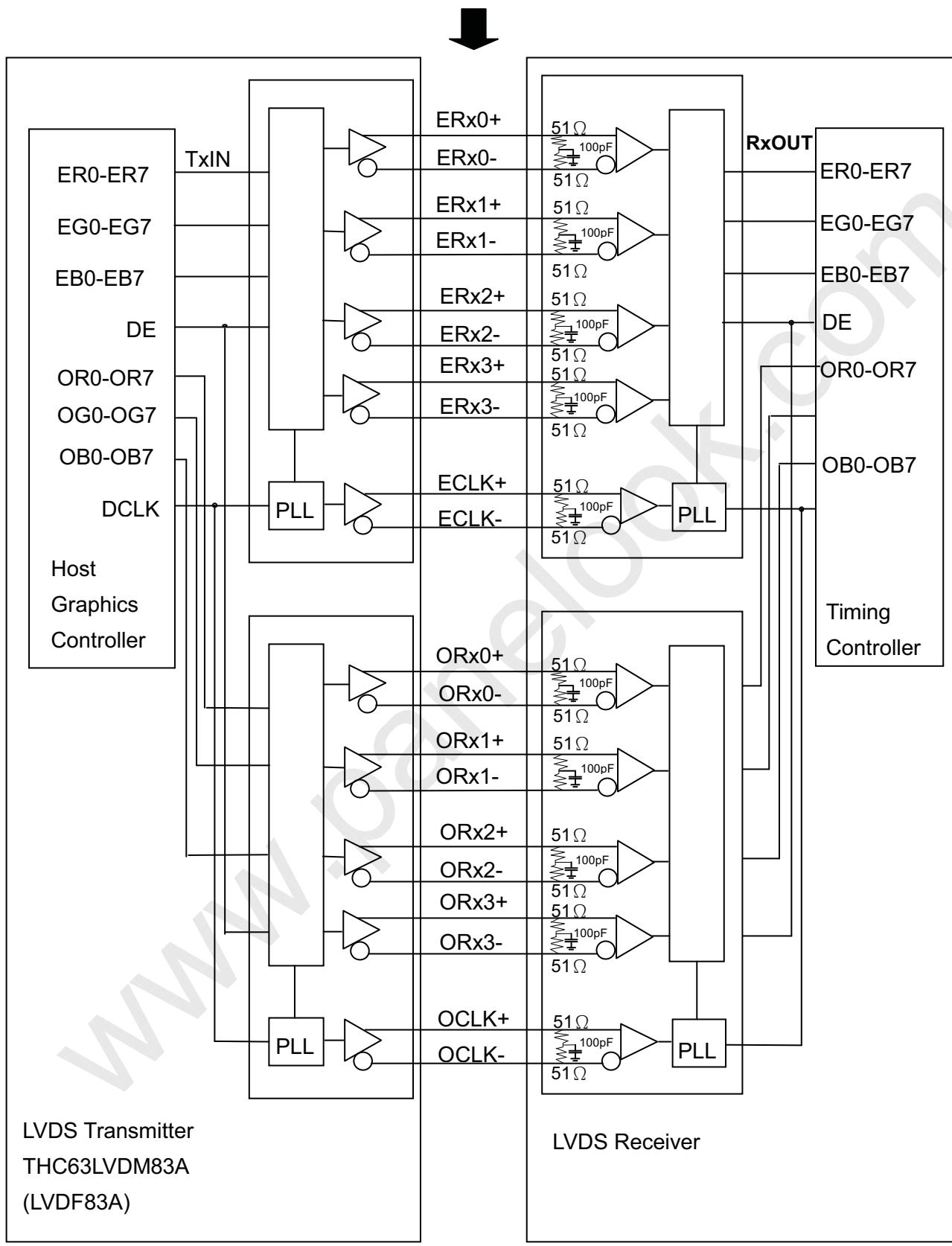
CN1(Header): S14B-PH-SM4-TB (JST) or CI0114M1HR0-LA (CviiLux)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

## Notice

1. If Pin14 is open, E\_PWM is 100% duty.

## 5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

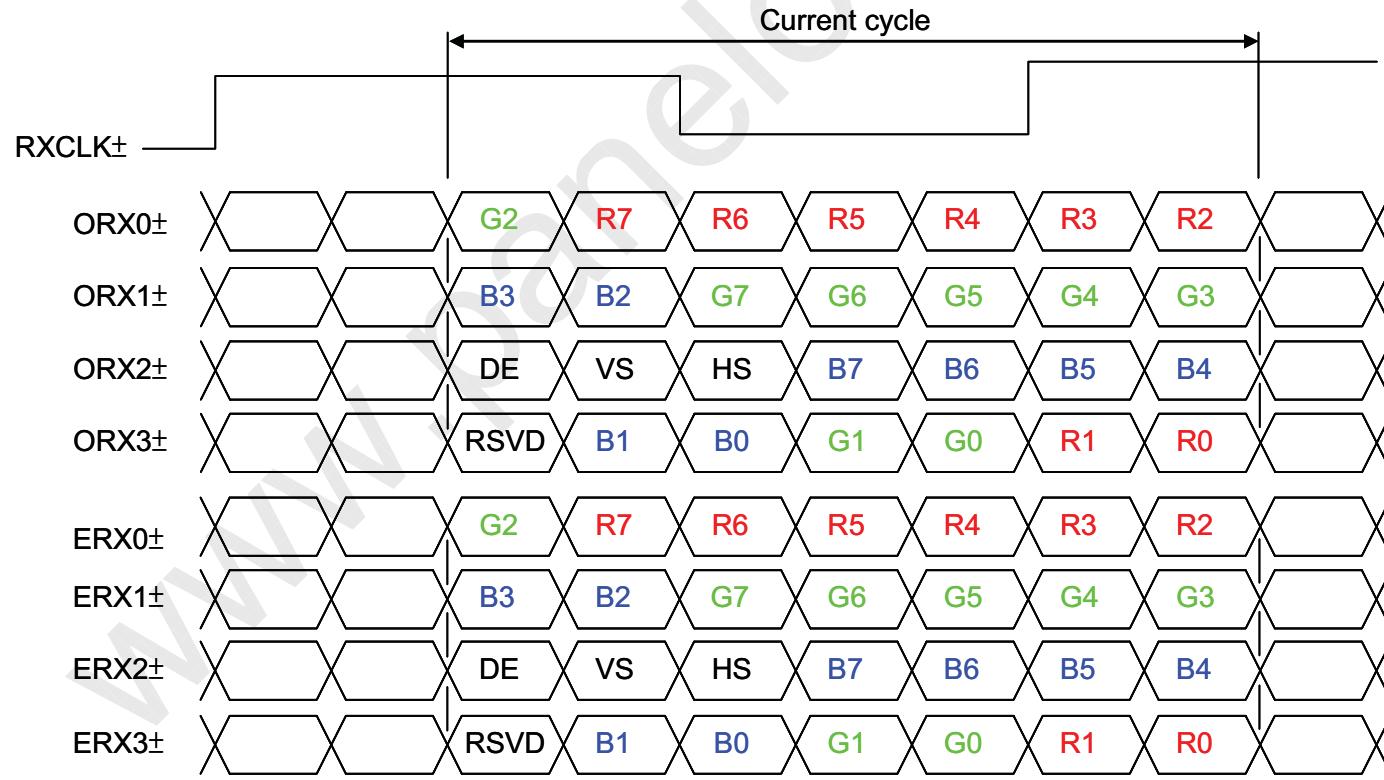
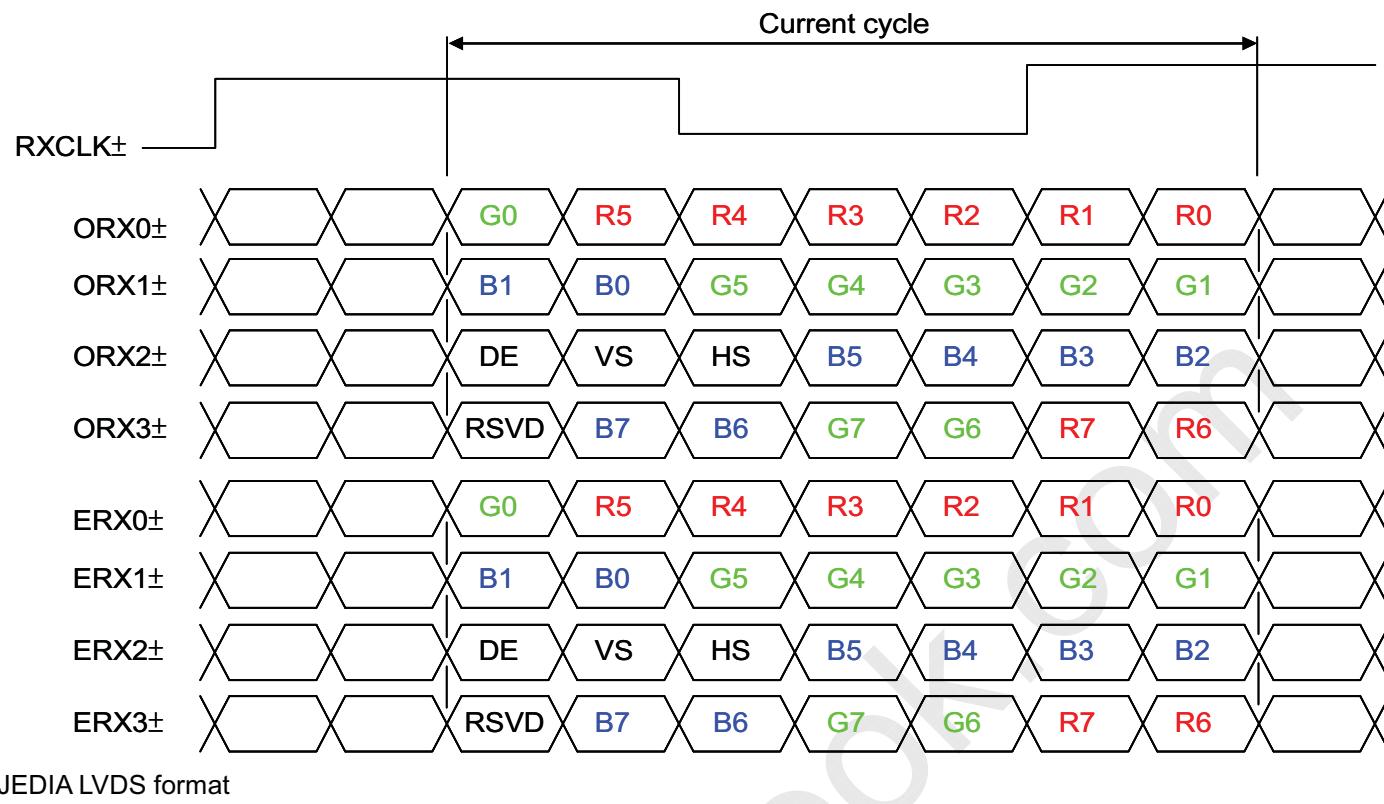
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

## 5.5 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format



## 5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color.

The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Red (253)	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (254)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (255)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	0	1	1	1	1	1	1	1	0	1	0	0	0	0		
	Green (253)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	Green (254)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	Green (255)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	
	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
Gray Scale Of Blue	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:	:	:	:	:	:	:	:	:	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

## 6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{\text{clkin}}$ (=1/TC)	60	74.25	77	MHz	
	Input cycle to cycle jitter	$T_{\text{rcl}}$	-	-	200	ps	(2)
	Spread spectrum modulation range	$F_{\text{clkin\_mod}}$	$F_{\text{clkin}}-2\%$	-	$F_{\text{clkin}}+2\%$	MHz	(3)
	Spread spectrum modulation frequency	$F_{\text{SSM}}$	-	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSKM	-400	-	400	ps	(4)

## 6.1.1 Timing spec for Frame Rate = 50Hz

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note	
Frame rate	2D mode	$F_{\text{r5}}$	47	50	53	Hz		
	3D mode	$F_{\text{r5}}$	50	50	50	Hz	(6)	
Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1380	Th	$Tv=Tvd+Tvb$
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	35	45	300	Th	—
	3D Mdoe	Total	Tv	1350			Th	(5), (7)
		Display	Tvd	1080			Th	
		Blank	Tvb	270			Th	
Horizontal Active Display Term	2D Mode	Total	Th	1050	1100	1150	Tc	$Th=Thd+Thb$
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—
	3D Mdoe	Total	Th	1050	1100	1150	Tc	$Th=Thd+Thb$
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	90	140	190	Tc	—

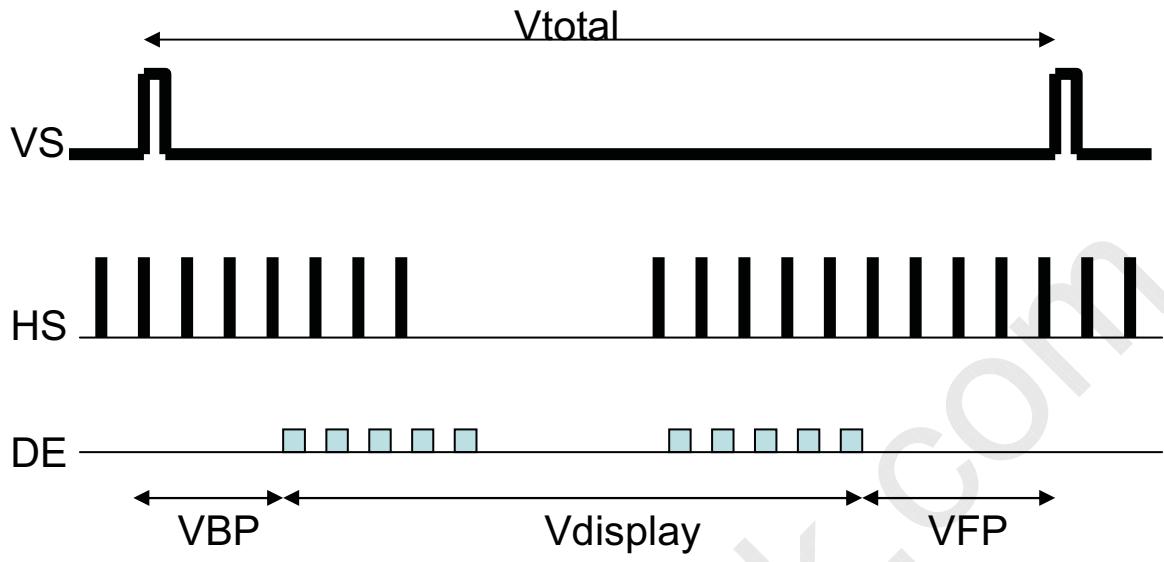
## 6.1.2 Timing spec for Frame Rate = 60Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		$F_{r6}$	57	60	62.5	Hz	
	3D mode		$F_{r6}$	60	60	60	Hz	(6)
Vertical Active Display Term	2D Mode	Total	$Tv$	1115	1125	1380	Th	$Tv=Tvd+Tv_b$
		Display	$Tvd$	1080	1080	1080	Th	—
		Blank	$Tvb$	35	45	300	Th	—
	3D Mode	Total	$Tv$	1125			Th	(5), (7)
		Display	$Tvd$	1080			Th	
		Blank	$Tvb$	45			Th	
Horizontal Active Display Term	2D Mode	Total	$Th$	1050	1100	1150	$Tc$	$Th=Thd+Th_b$
		Display	$Thd$	960	960	960	$Tc$	—
		Blank	$Th_b$	90	140	190	$Tc$	—
	3D Mode	Total	$Th$	1050	1100	1150	$Tc$	$Th=Thd+Th_b$
		Display	$Thd$	960	960	960	$Tc$	—
		Blank	$Th_b$	90	140	190	$Tc$	—

Note (1) Please make sure the range of pixel clock has follow the below equation:

$$F_{Clkin(max)} \geq F_{r6} \times Tv \times Th$$

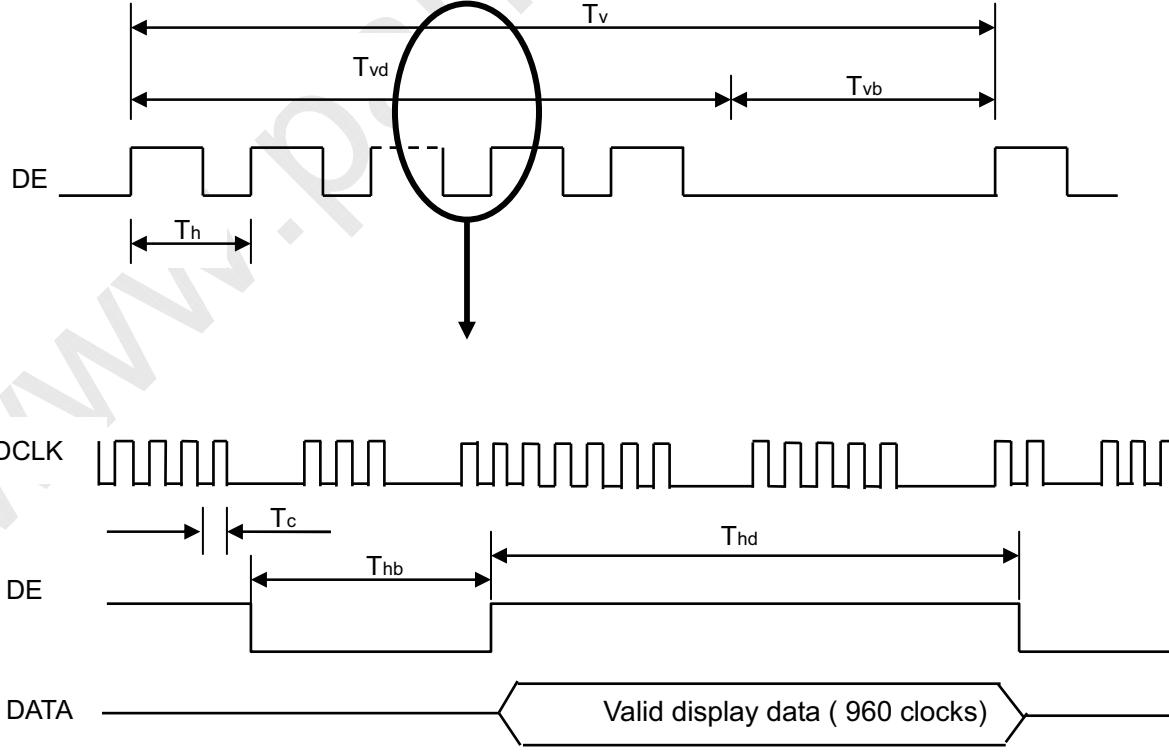
$$F_{r5} \times Tv \times Th \geq F_{Clkin(min)}$$

INPUT SIGNAL TIMING DIAGRAM

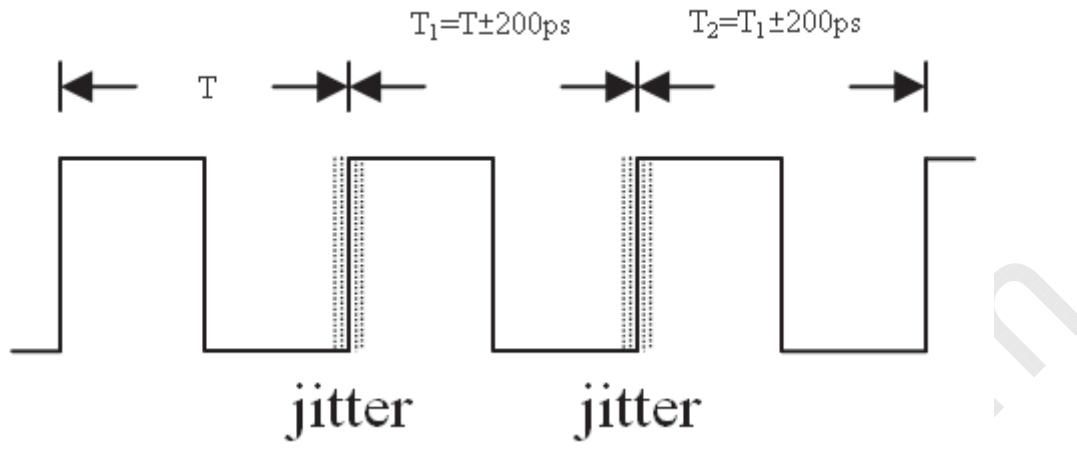
- VBP max : 150 line

Suggest VBP = VFP =  $\frac{1}{2} * (V_{total} - V_{display})$

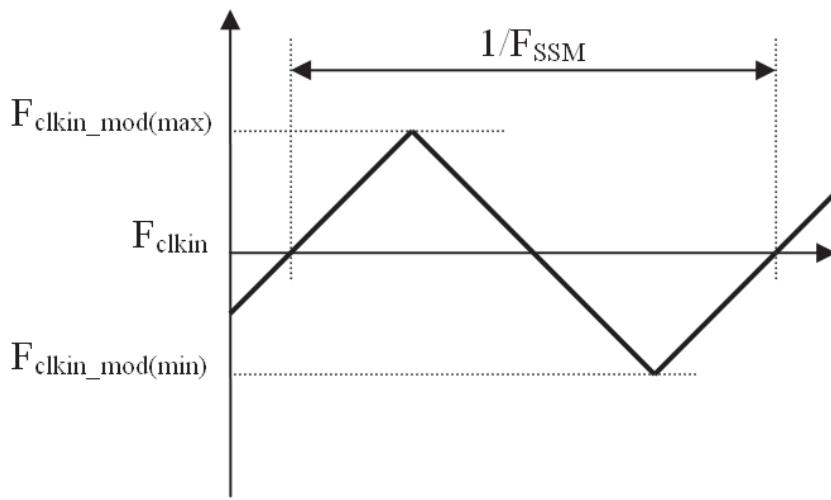
DE timing



Note (2) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_2|$

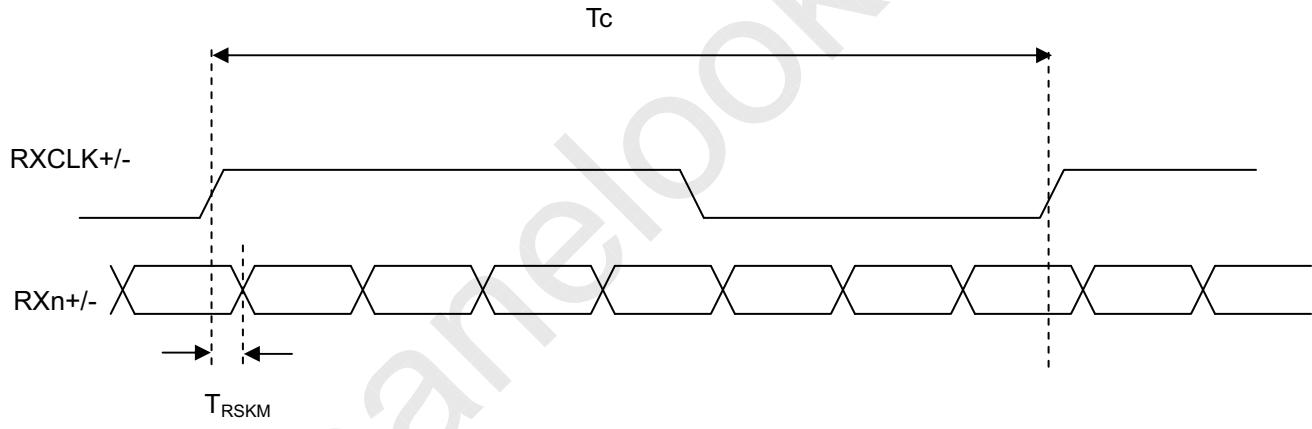


Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (4) LVDS receiver skew margin is defined and shown as below

**LVDS RECEIVER INTERFACE TIMING DIAGRAM**



Note (5) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 50Hz 3D mode and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 60Hz 3D mode

Note (6) In 3D mode, the set up Fr5 and Fr6 in Typ.  $\pm 3$  Hz .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

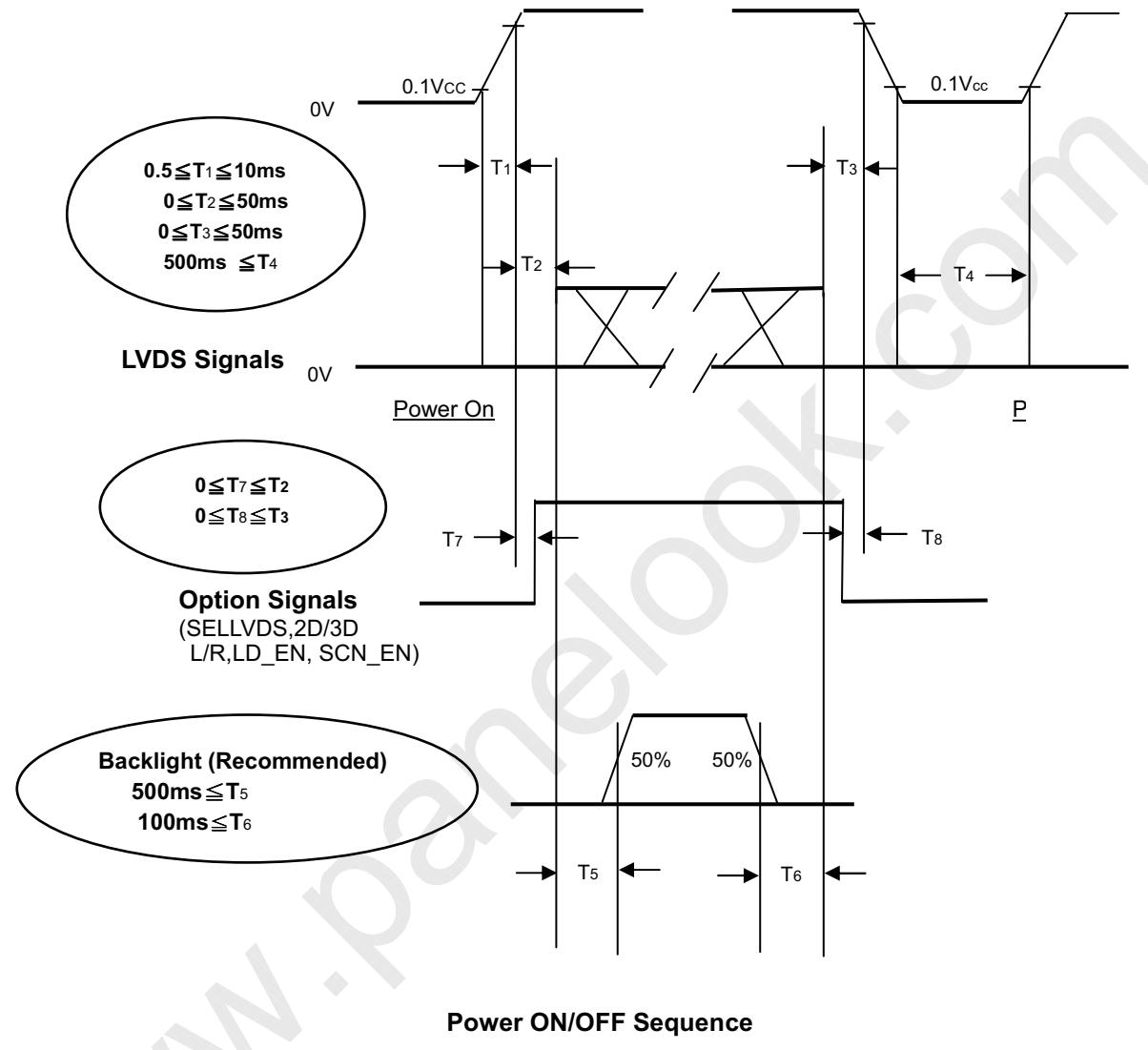
Note (7) In 3D mode, the set up Tv and Tvb in Typ.  $\pm 30$ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

## 6.2 POWER ON/OFF SEQUENCE

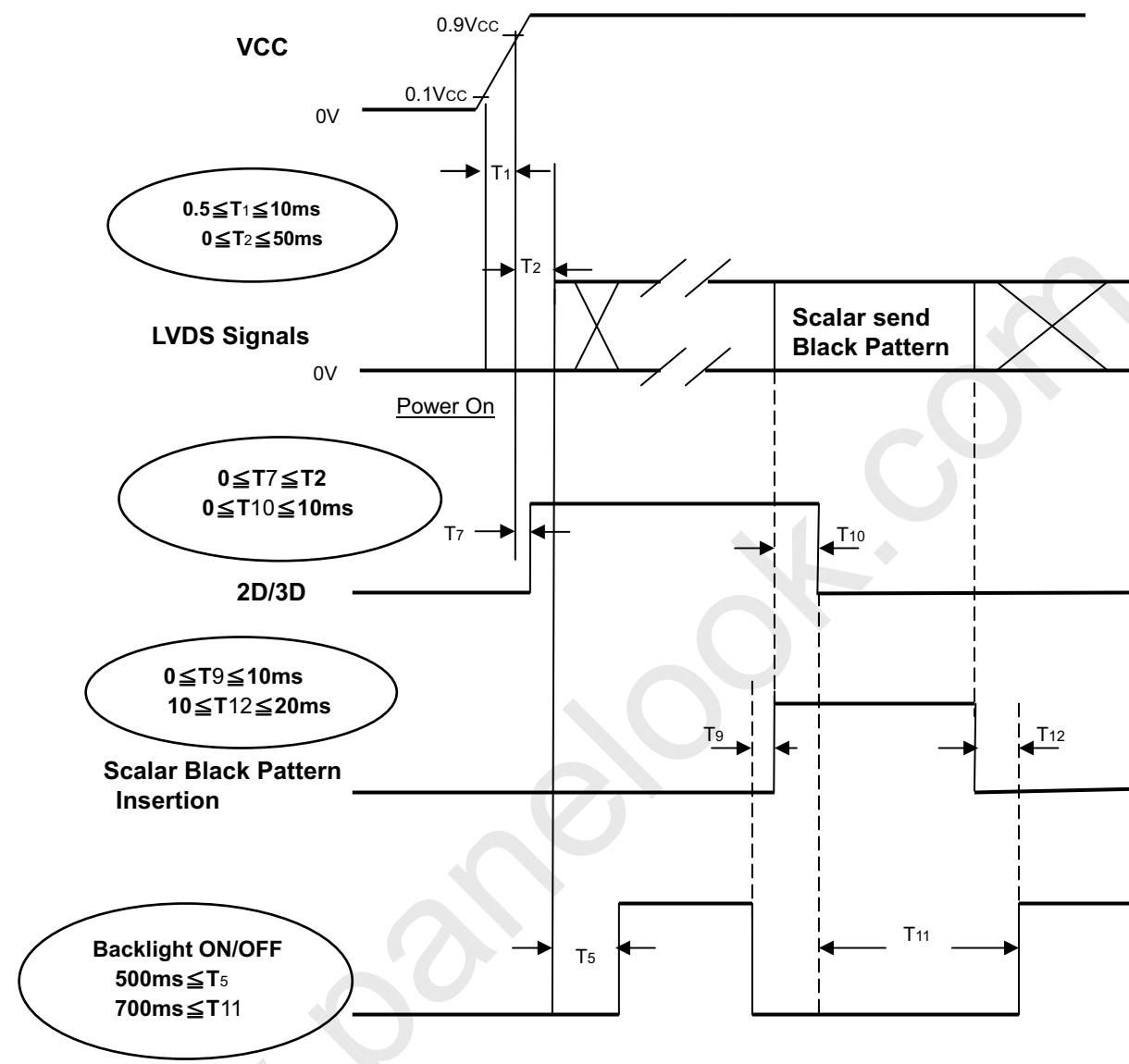
( $T_a = 25 \pm 2 {}^\circ\text{C}$ )

### 6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



## 6.2.2 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If  $T_2 < 0$ , that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

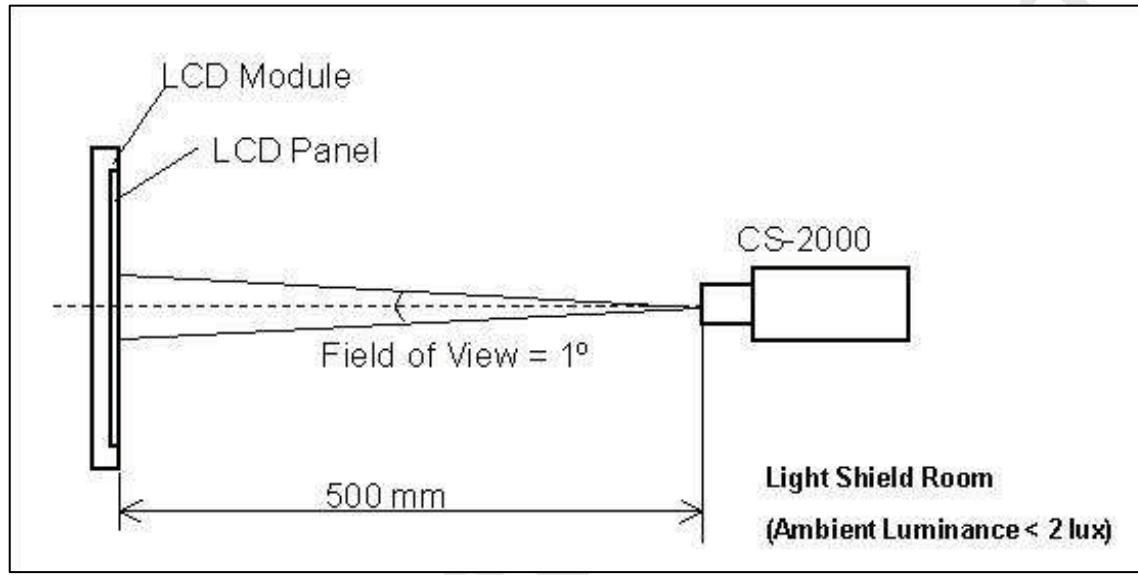
Note (7) 2D/3D switching time should be larger than 500ms.

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	T <sub>a</sub>	25±2	°C
Ambient Humidity	H <sub>a</sub>	50±10	%RH
Supply Voltage	V <sub>CC</sub>	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I <sub>L</sub>	115	mA

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. "42")



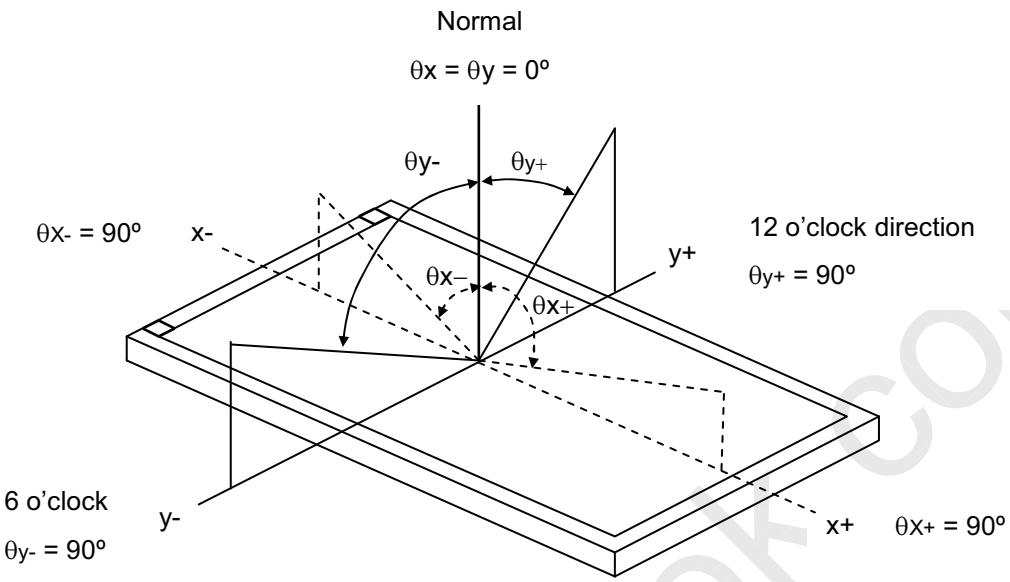
## 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing angle at normal direction	3500	5000	-	-	Note (2)	
Response Time	Gray to gray			6	12	ms	Note (3)	
Center Luminance of White	$L_C$		320	400	-	cd/m <sup>2</sup>	Note (4)	
				85	-	cd/m <sup>2</sup>	Note (8)	
White Variation	$\delta W$				1.3	-	Note (6)	
Cross Talk	CT		-	-	4	%	Note (5)	
			-	4	-	%	Note (8)	
			-	11	-	%	Note (8)	
Color Chromaticity	Red	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing angle at normal direction	0.645	Typ.-0.03	-	-	(1)	
			0.330		-	-		
	Green		0.300		-	-		
			0.595		-	-		
	Blue		0.145		-	-		
			0.055		-	-		
	White		0.280	Typ.+0.03	-	-		
			0.290		-	-		
	Correlated color temperature		9800		K	-		
	Color Gamut	C.G.	-		72	-	% NTSC	
Viewing Angle	Horizontal	$CR \geq 20$	80	88	-	Deg. (1)	(1)	
			80	88	-			
	Vertical		80	88	-			
			80	88	-			
Transmission direction of the up polarizer	$\Phi_{up-P}$				90		Deg. (7)	

Note (1) Definition of Viewing Angle ( $\theta_x$ ,  $\theta_y$ ):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

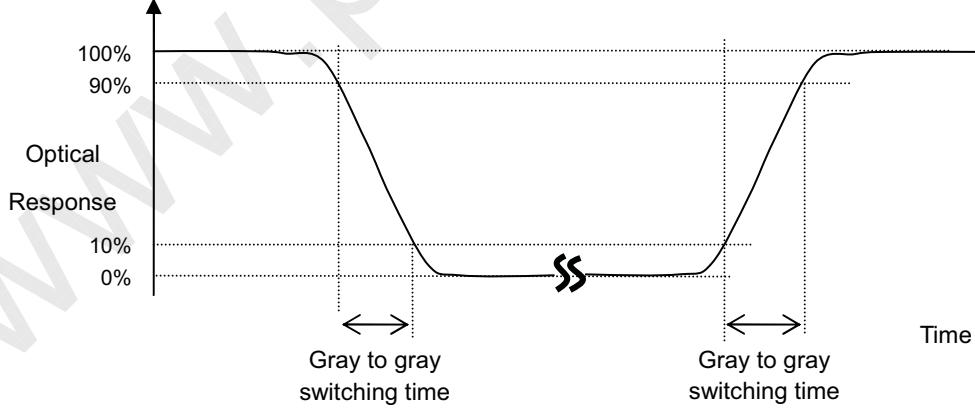
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

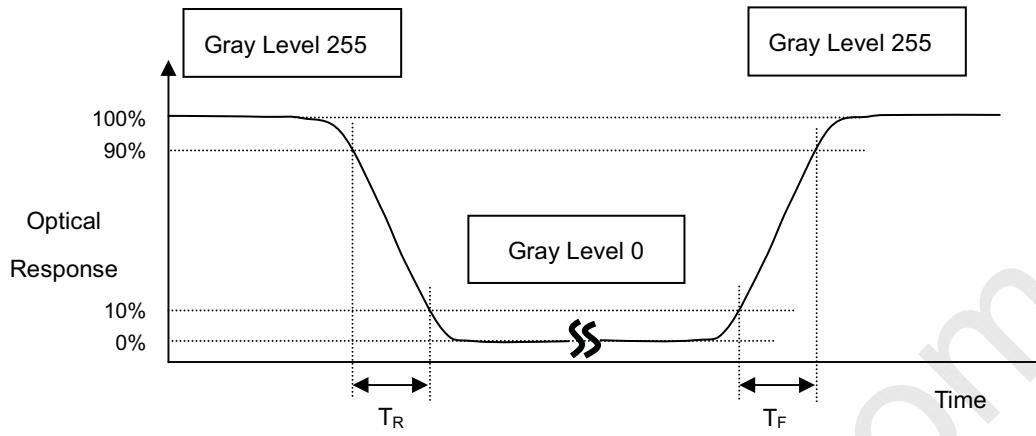
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Definition of Response Time ( $T_R$ ,  $T_F$ ):



Note (4) Definition of Luminance of White ( $L_C$ ):

Measure the luminance of gray level 1023 at center point.

$L_C = L(5)$ , where  $L(x)$  is corresponding to the luminance of the point X at the figure in Note (6).

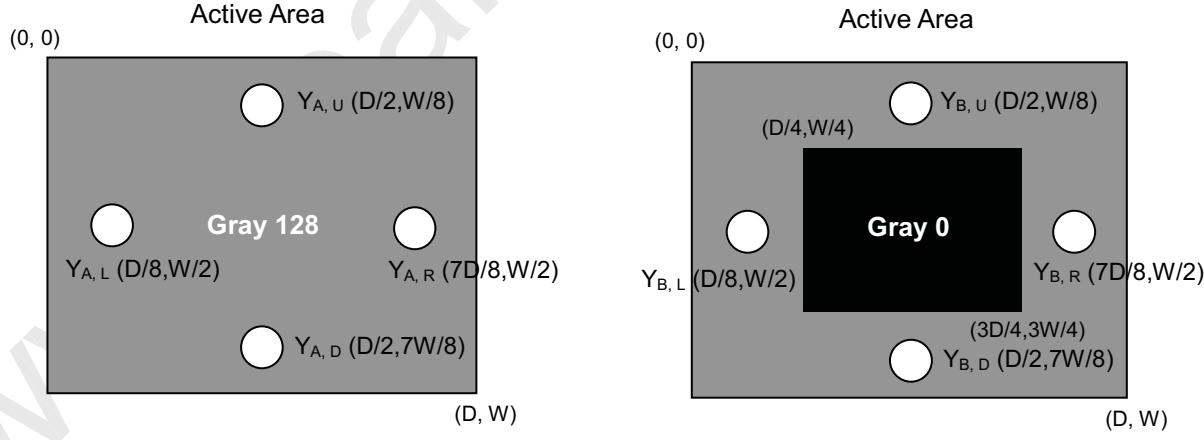
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

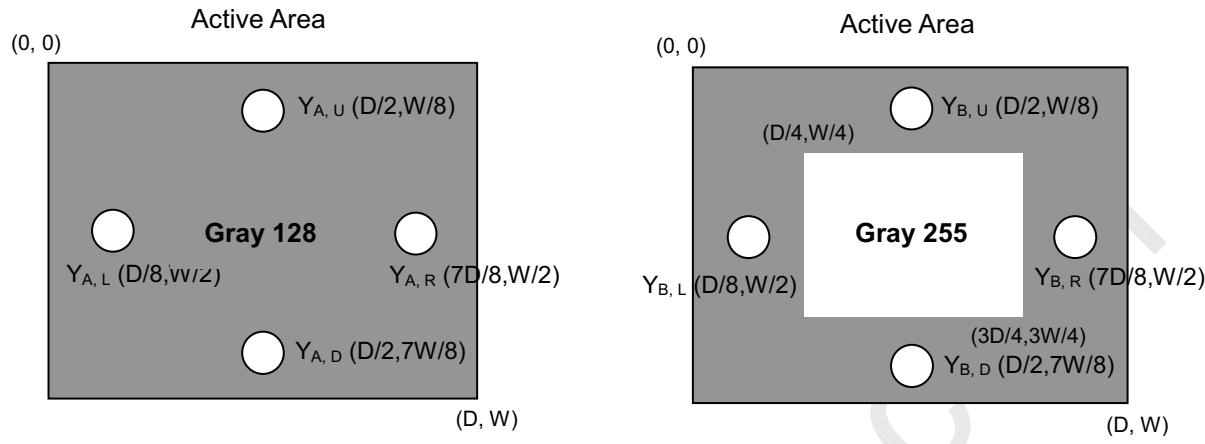
$Y_A$  = Luminance of measured location without gray level 0 pattern ( $cd/m^2$ )

$Y_B$  = Luminance of measured location with gray level 0 pattern ( $cd/m^2$ )



YA = Luminance of measured location without gray level 255 pattern (cd/m<sup>2</sup>)

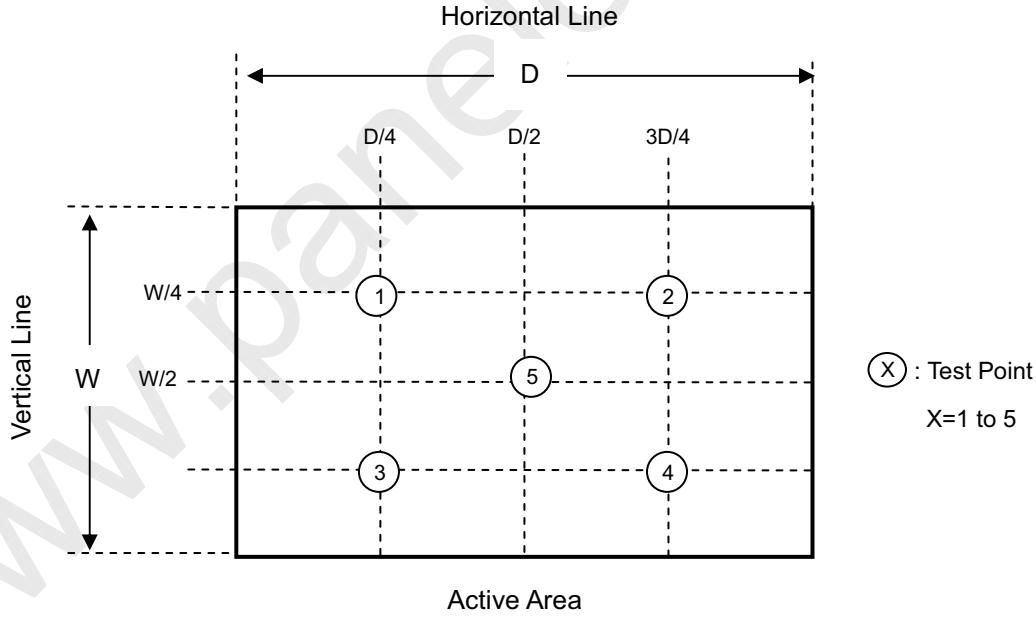
YB = Luminance of measured location with gray level 255 pattern (cd/m<sup>2</sup>)



Note (6) Definition of White Variation ( $\delta W$ ):

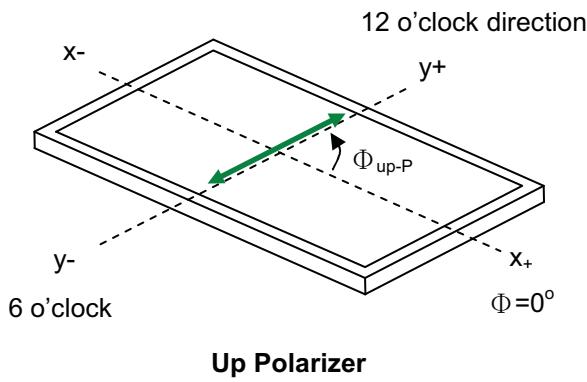
Measure the luminance of gray level 255 at 5 points

$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$

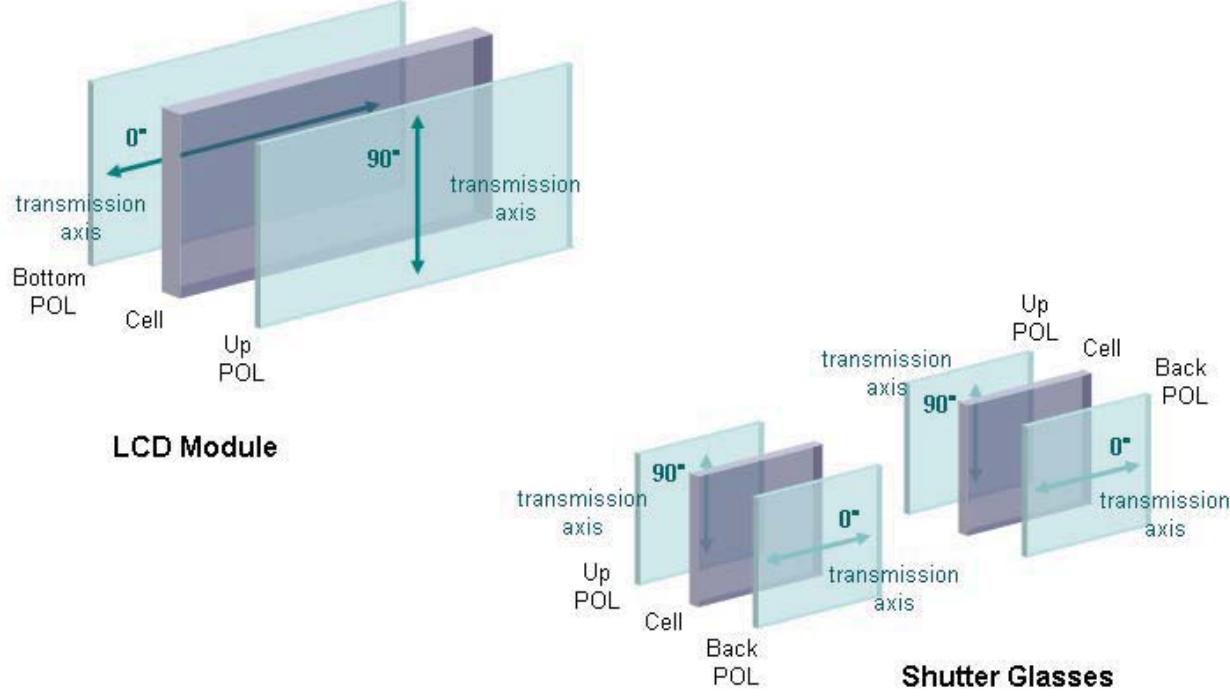


Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer( $\Phi_{up-P}$ ) on LCD Module:



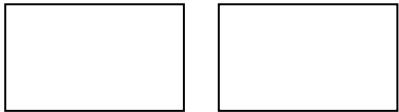
The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



Note(8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

a. Test pattern

Left eye image and right eye image are displayed alternated



WW

Left eye image: W255; Right eye image: W255



WB

Left eye image: W255; Right eye image: W0



BW

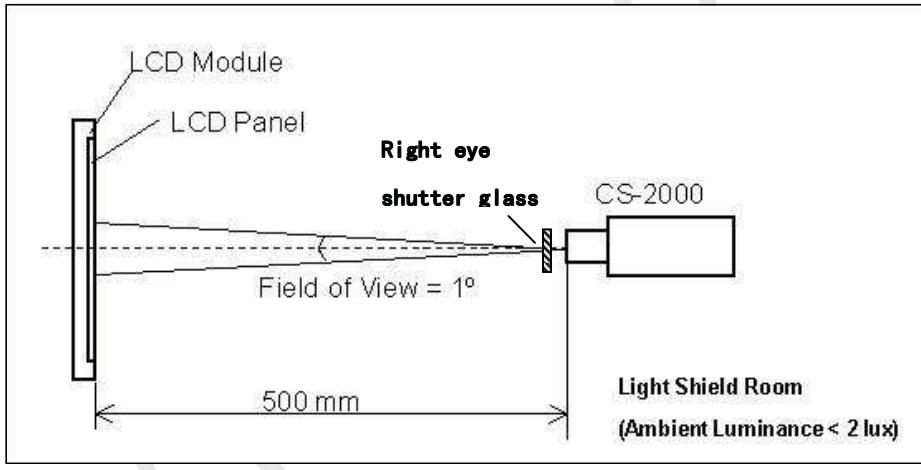
Left eye image: W0; Right eye image: W255



BB

Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted  $L(WW)$ ; the luminance of the test pattern "WB", denoted  $L(WB)$ ; the luminance of the test pattern "BW", denoted  $L(BW)$ ; the luminance of the test pattern "BB", denoted  $L(BB)$

c. Definition of the Center Luminance of White,  $L_c(3D)$  :  $L(WW)$

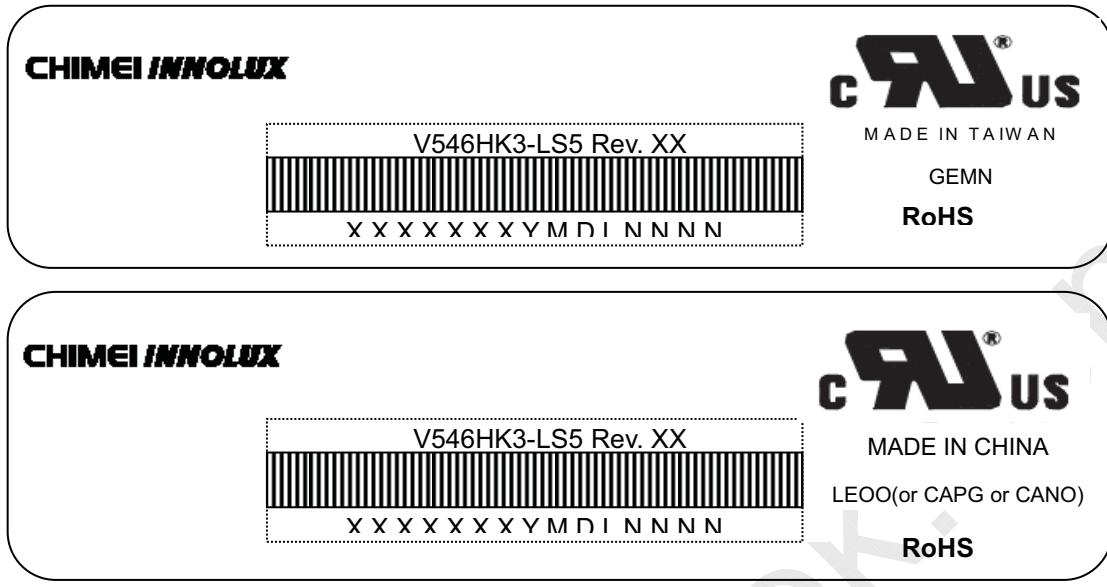
d. Definition of the 3D mode white crosstalk,  $CT(3D-W)$  :  $CT(3D-W) = \left| \frac{L(WB) - L(BB)}{L(WW) - L(BB)} \right|$

e. Definition of the 3D mode dark crosstalk,  $CT(3D-D)$  :  $CT(3D-D) = \left| \frac{L(WW) - L(BW)}{L(WW) - L(BB)} \right|$

## 8. DEFINITION OF LABELS

### 8.1 CMI MODULE LABEL

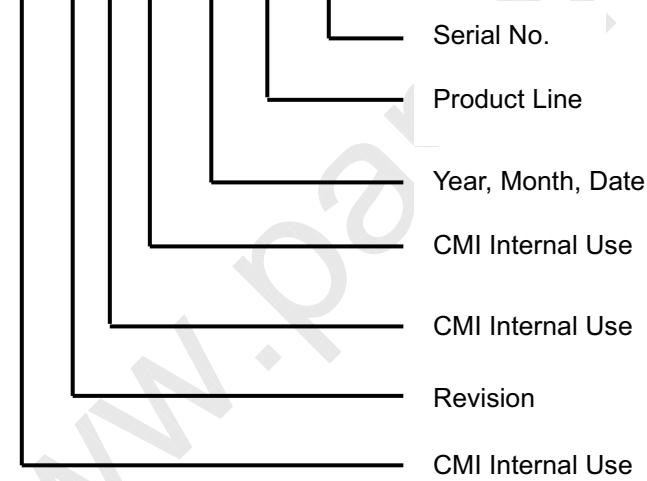
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V546H1-LS2

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

## 9. Packaging

### 9.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules / 1 Box
- (2) Box dimensions: 1334(L) X 284 (W) X 856 (H)
- (3) Weight: approximately 48Kg (3 modules per box)

### 9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

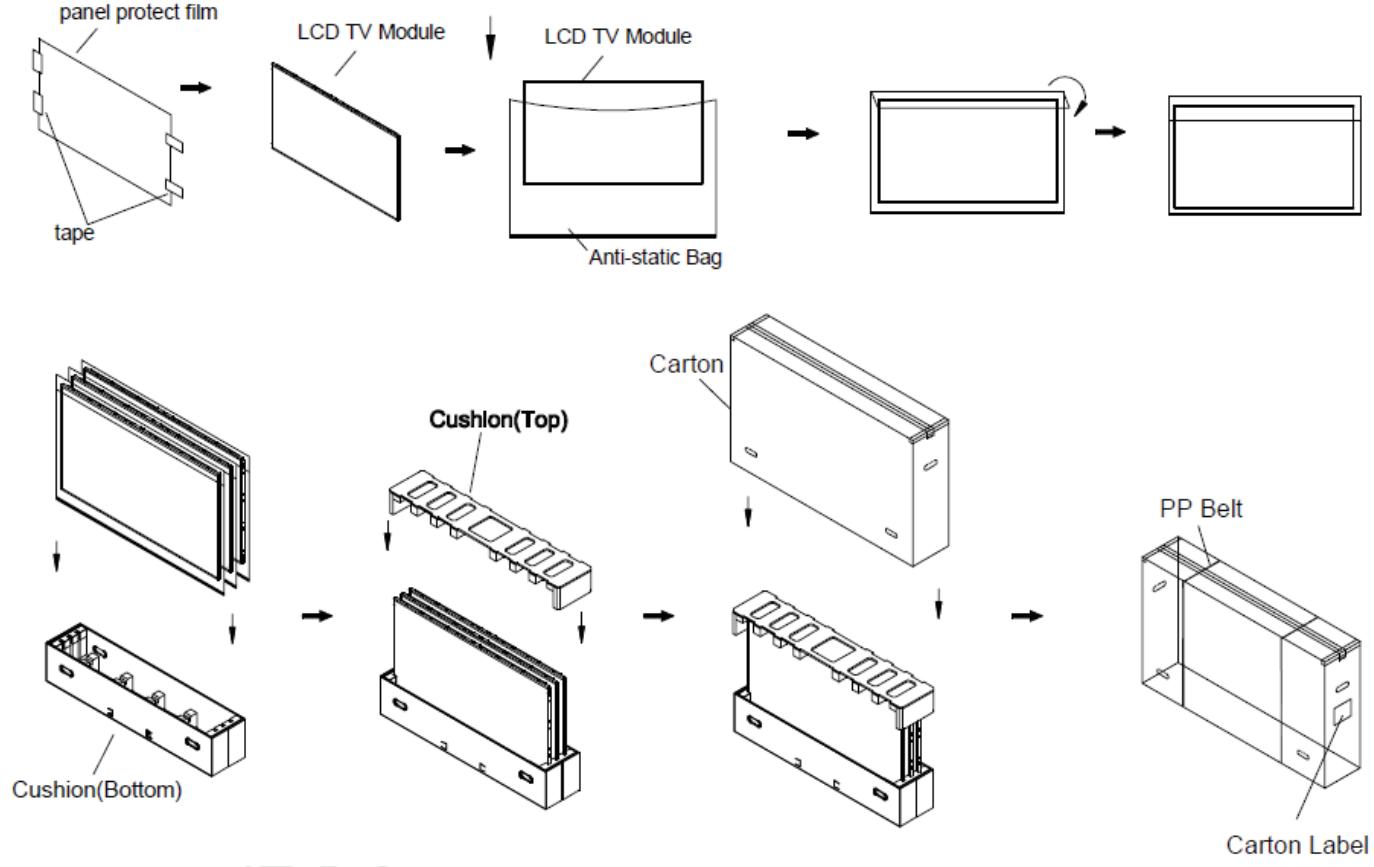


Figure.9-1 packing method

Sea / Land Transportation (40ft &amp; 40ft HC)

Figure. 9-2 Packing method

Air Transportation

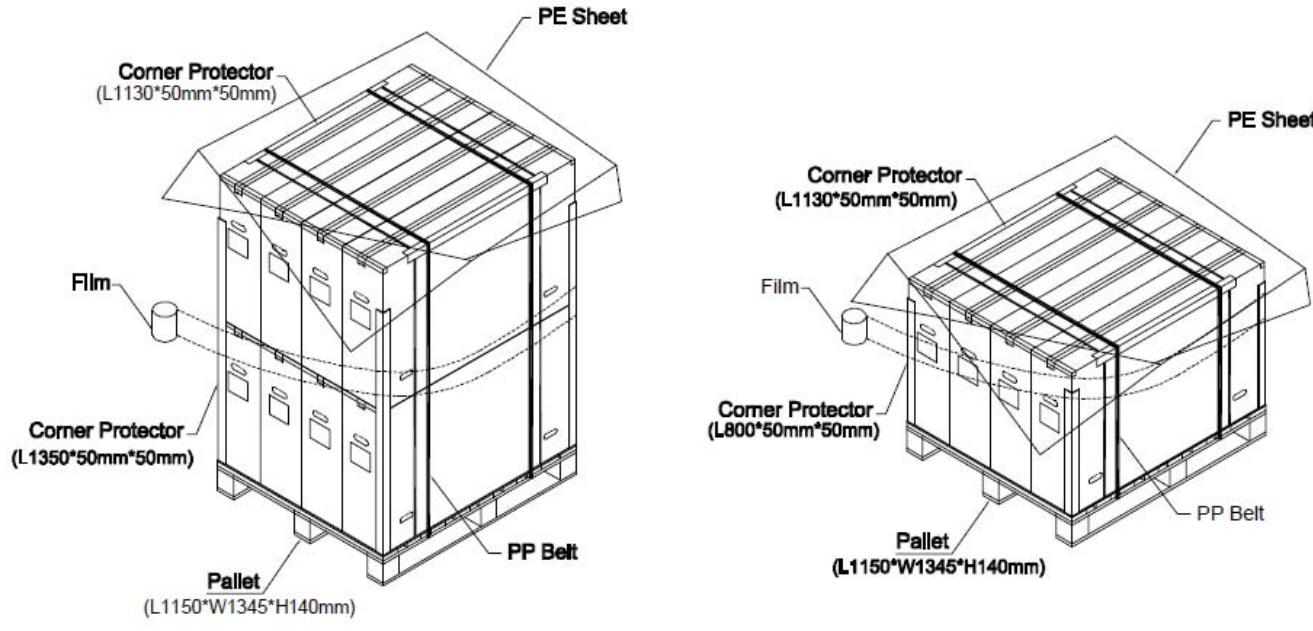


Figure. 9-2 Packing method

**10. Internal Standard****10.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) UL 60950-1, UL 60065: Standard for Safety of Information Technology Equipment Including electrical Business Equipment.
- (2) IEC 60950-1:2005, IEC 60065:2001+ A1:2005 ; Standard for Safety of International Electrotechnical Commission.
- (3) EN 60950-1:2006+ A11:2009, EN60065:2002 + A1:2006 + A11:2008; European Committee for Electrotechnical Standardization (CENELEC), EUROPEAN STANDARD for Safety of Information Technology Equipment Including Electrical Business Equipment.

**10.2 EMC**

- (1) ANSI C63.4 Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electrical Equipment in the Range of 9kHz to 40GHz. " American National standards Institute(ANSI)
- (2) C.I.S.P.R " Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment. " International Special committee on Radio Interference.
- (3) EN 55022 " Limits and Methods of Measurement of Radio Interface Characteristics of Information Technology Equipment. " European Committee for Electrotechnical Standardization.(CENELEC)

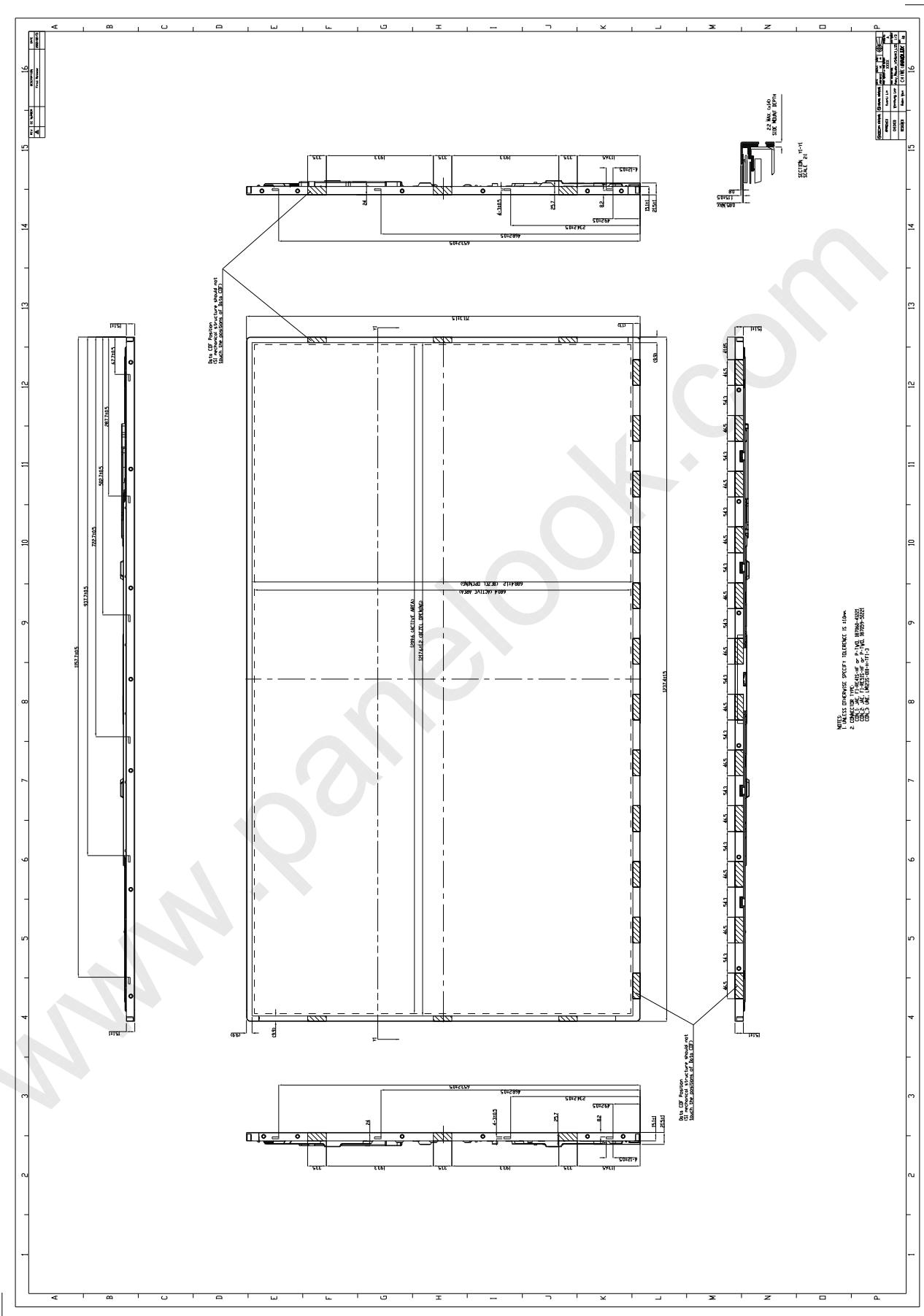
**11. PRECAUTIONS****11.1 ASSEMBLY AND HANDLING PRECAUTIONS**

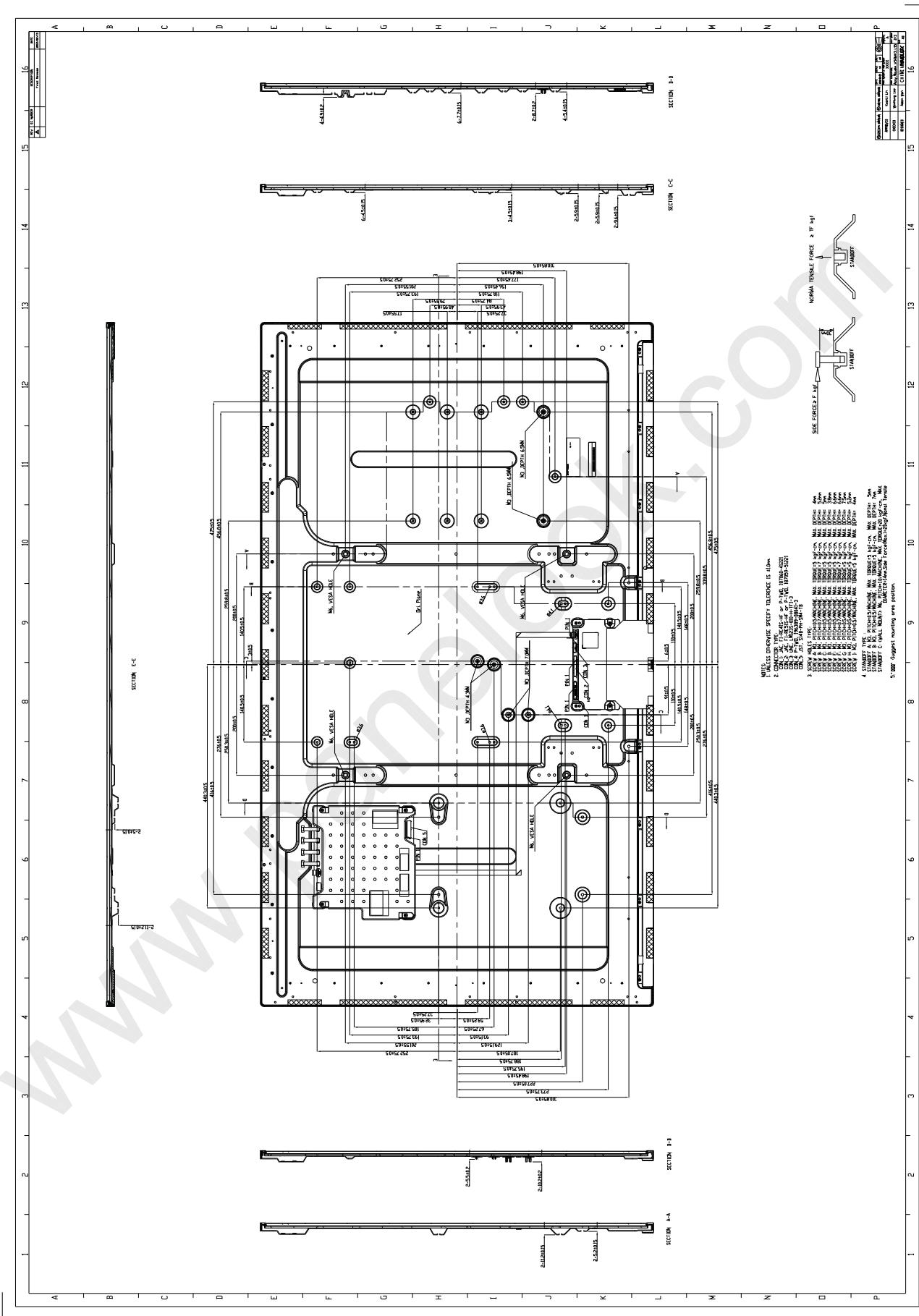
- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

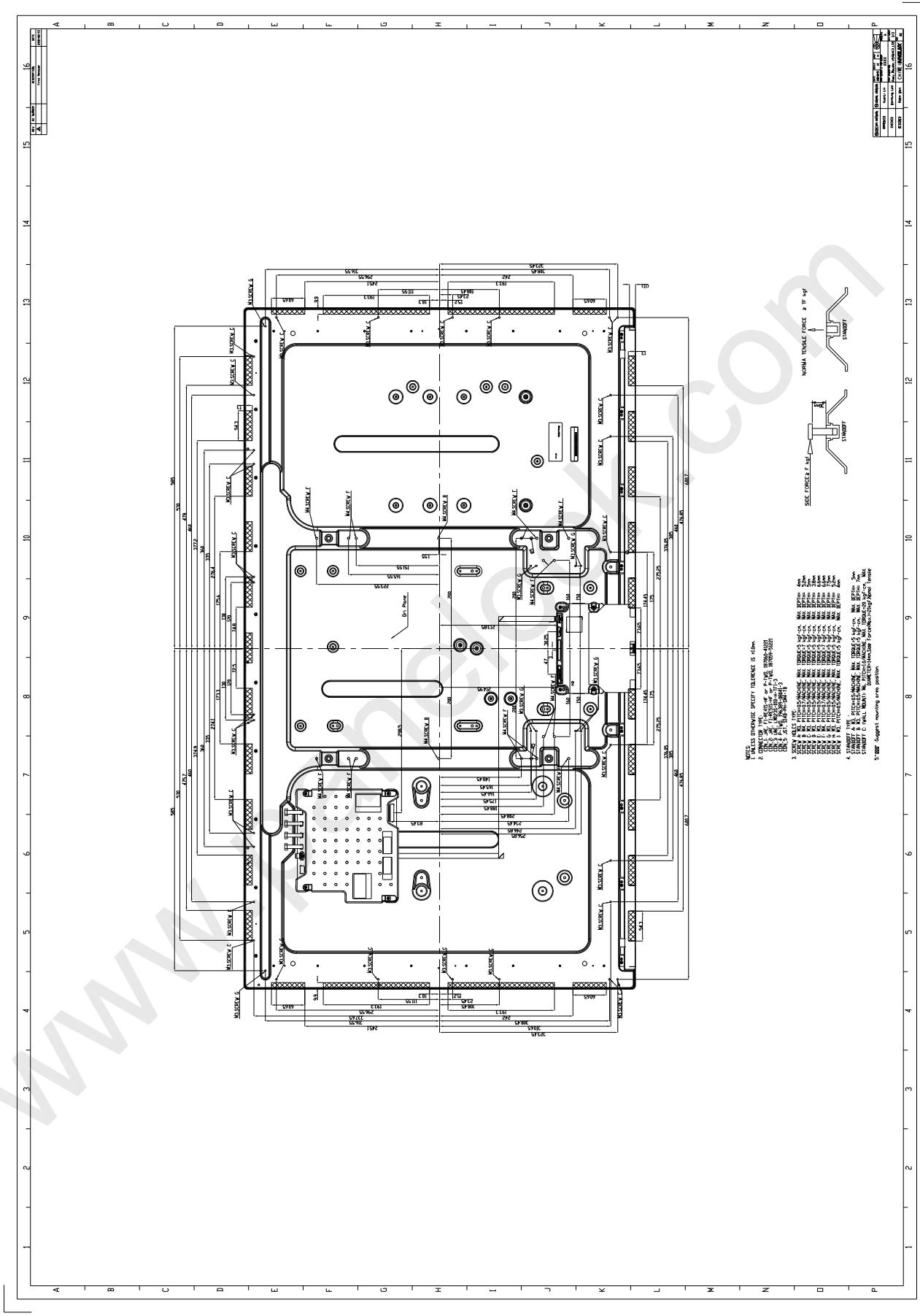
**11.2 SAFETY PRECAUTIONS**

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

## 12. MECHANICAL CHARACTERISTIC







## Appendix A

## Local Dimming demo function

## A.1 I2C address and write command

Device address: 0xe0

Register address: 0x65

Command data: 0x16 0x00 0x00 0x00 0x00 0x00: Local Dimming demo mode OFF (Note 1)

0x16 0x00 0x00 0x00 0x00 0x01: Local Dimming demo mode ON (Demo in right half screen) (Note 2)

Preamble data: 0x26 0238

I2C data:

Device Address

Preamble data

Preamble data

START	11100000 (0xE0)	ACK	00100110 (0x26)	ACK	00111000 (0x38)	ACK
-------	--------------------	-----	--------------------	-----	--------------------	-----

Register Address

Command Data

Command Date

01100101 (0x65)	ACK	00010110 (0x16)	ACK	00000000 (0x00)	ACK
--------------------	-----	--------------------	-----	--------------------	-----

Command Date

Command Data

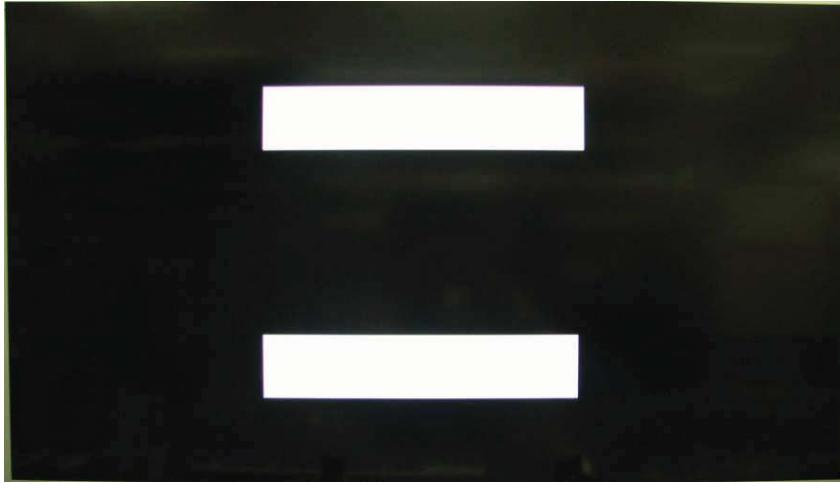
Command Date

00000000 (0x00)	ACK	00000000 (0x00)	ACK	00000000 (0x00)	ACK
--------------------	-----	--------------------	-----	--------------------	-----

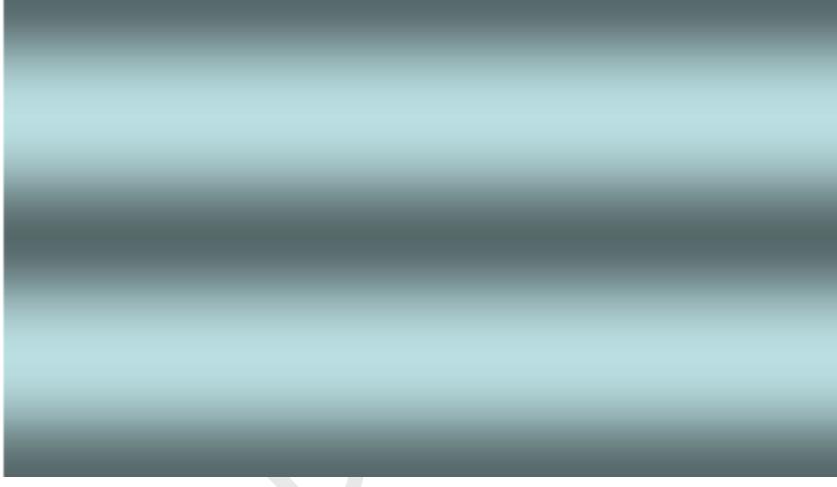
Command Date

00000001 (0x01)	STOP
--------------------	------

Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



## A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
$t_{SU-STA}$	Start setup time	250	-	ns
$t_{HD-STA}$	Start hold time	250	-	ns
$t_{SU-DAT}$	Data setup time	80	-	ns
$t_{HD-DAT}$	Data hold time	0	-	ns
$t_{SU-STO}$	Stop setup time	250	-	ns
$t_{BUF}$	Time between Stop condition and next Start condition	500	-	ns

